Mask Set Errata for Mask 0N35F

This report applies to mask 0N35F for these products:

- S08PT16 S08PA16 S08PT8 S08PA8

Errata ID	Errata Title
6657	ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2
5264	DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address
5265	DBG: DGB can not store data into FIFO when writing data to RAM and/or flash space at Event B only trigger mode or A then event only B trigger mode
5266	DBG: source address of BSR instruction stored in FIFO instead of the destination address
6251	NVM: flash commands might not run due to an unexpected protection violation
6245	NVM: flash protection issue affecting program flash command
2793	I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched
5288	ICS: ICS_S[LOCK] flag not set after wakeup from stop mode when BDM mode is enabled
7331	IO: High current drive pins not in high-Z state during power up
4592	PMC: Unstable to wake up MCU from stop3 mode with LVD disabled when the MCU power supply VDD is in the low range
4567	PMC: higher stop3 IDD after power on reset
7891	Port: both PTB6 and PTB7 pins can not function as open-drain when configured as IIC function
7040	SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

e6657: ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2

Errata type: Errata
Description: When the ADC FIFO mode is enabled, the FIFO can not get correct result if the bus clock is slower than ADC conversion clock divided by 2.

Workaround: Configure the bus clock to be faster than the ADC conversion clock (ADCK) divided by 2 if the ADC FIFO is used.

e5264: DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address

Errata type: Errata

Description: When setting breakpoint at the address other than instruction opcode address, the comparator C with TAG type can not generate breakpoint. This issue does not affect code execution.

Workaround: If such tag breakpoint at the address other than instruction opcode address is required, use comparator A and/or B tag breakpoint.

e5266: DBG: source address of BSR instruction stored in FIFO instead of the destination address

Errata type: Errata

Description: In COF storing mode, the address stored in FIFO for a BSR instruction is the source address instead of the destination address.

Workaround: No workaround.

e6251: NVM: flash commands might not run due to an unexpected protection violation

Errata type: Errata

Description: In the protection scenario 1, if bits FPHS[1:0] are set to '11' the user might expect that it would behave the same as scenario 3 (flash fully unprotected). However, in such a configuration in scenario 1 the commands that affect the whole flash array (Erase flash block, Erase all block, Unsecure flash) will not execute and flag PVIOL will set indicating a protection violation.

Workaround: In order to launch the commands that affect the whole flash array protection must be set according to scenario 3 (flash fully unprotected).

e6245: NVM: flash protection issue affecting program flash command

Errata type: Errata

Description: There is a problem affecting program flash command in a scenario where the flash is partially protected.

When program flash command is used to program 8-bytes, starting from the address that corresponds to the last 4-bytes in the flash unprotected region (therefore crossing the boundary into the protected region), the program flash command will program the full set of 8 bytes: 4 bytes in the unprotected region and the next 4 bytes in the protected region, what results in an undetected protection violation.

Workaround: The application should launch program flash command to program 4-bytes or 8-bytes to correctly match the limits of the flash unprotected region, not forcing the transition from the unprotected to the protected region as explained above.

e2793: I2C: MCU does not wake as expected from STOP mode on subsequent address matches if previous address is mismatched

Errata type: Errata

Description: The I2C module, acting as a slave on the I2C bus, does not wake as expected from normal STOP mode on a valid address match if the previous address was not a match.

When the external I2C master sends a non-matching address, the I2C slave state machine does not look for a start bit past the first start bit on the bus. Consequently, subsequent transmissions by the I2C master with a matching address do not, on the first matching address, wake the MCU from STOP mode via the I2C interrupt.

Workaround: There are multiple workarounds:

(1) The master must continually re-transmit the MCU's slave address upon not receiving a NACK from the slave device during the slave addressing phase of the transmission. For clarification, the master must perform the following:

a) Send slave device address

b) Check for ACK bit

c) If ACK was received, continue with data transmission. Else, send repeated start signal and repeat steps a-c.

NOTE: Due to the nature of the errata, the maximum number of retransmissions needed to wake the part is nine times.

(2) When the MCU, operating as an I2C slave, is in STOP mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves. The user must also ensure that MCU does not return to STOP until after all packets to non-matching addresses have been sent.

(3) Use a pin interrupt (any pin, whether that pin is or is not being used by the active I2C module) to wake up the part before receiving I2C packets. NOTE: If using the SDA or SCL pin that the active I2C module is using, the part will wake-up on every I2C transaction on the bus.

(4) Use Wait mode instead of STOP mode.

e5288: ICS: ICS_S[LOCK] flag not set after wakeup from stop mode when BDM mode is enabled

Errata type: Errata

Description: ICS_S[LOCK] flag can not be set after wakeup from stop mode when BDM mode is enabled. This can be observed during code debugging with CodeWarrior when the debugger wakes up MCU via BDM. It does not affect code standalone execution.

Workaround: Perform two writes after wakeup from stop mode before checking LOCK flag:

1) write a different trim value than the manufacture default trim value to ICS_C3. The recommended value is default trim value + 1 or -1.

2) write the manufacture default trim value to ICS_C3.

e7331: IO: High current drive pins not in high-Z state during power up

Errata type: Errata

Description: The high current drive pins on the chip are unexpectedly driven low for a short period during power up. All other I/O pins are high impedance. The issue happens only before VDD reaches the power-on reset voltage. After power up the normal I/O functions on the high current drive pins are not impacted.

Workaround: Use one or more combination of the following methods to avoid possible issues:

- Use high current drive pins as current source for LED connection, but keep total IDD < 120mA (refer to device data sheet for IDD)
- Configure the corresponding Flextimer channel output polarity as active high which are muxed with high current drive pins
- Use high current drive pins with NPN transistor (active high) to drive relays
- Keep VDD ramp-up time greater than or equal to 1KV/s and less than or equal to 10KVs to disable LED and/or driver action during power up

e4592: PMC: Unstable to wake up MCU from stop3 mode with LVD disabled when the MCU power supply VDD is in the low range

Errata type: Errata

Description: The PMC does not provide enough current while waking up MCU from stop3 mode if the MCU power supply VDD is in the low range. If LVD enabled with LVDRE bit set and LVDSE bit clear, the LVD reset may occur with high MCU power supply VDD. The observed VDD can be as high as 4V when LVD reset on wakeup happens.

Workaround: The low power stop3 mode can only be used at VDD from 5V down to the high LVD trip (VLVDH) safely (4.2V to 5.5V). The low power stop3 mode cannot be used from 2.7V to 4.2V. High power stop3 mode (both LVDE bit and LVDSE bit set) can still be used for lower voltage applications.

It'll be fixed in future silicon revision.

e4567: PMC: higher stop3 IDD after power on reset

Errata type: Errata

Description: Abnormal high stop current is observed at cold temperature after power-on reset. It will take 1-2 seconds for stop current to drop to normal value (~3uA typical) from 100+uA at room temperature, 20 seconds at -20°C, up to a few minutes at -40°C. It will not be observed at hot temperature.

This issue does not affect applications which do not require stop3 mode. It'll be fixed in future silicon revision.

Workaround: It'll be fixed in future silicon revision.

e7891: Port: both PTB6 and PTB7 pins can not function as open-drain when configured as IIC function

Errata type: Errata

Description: When configured as the IIC function, the PTB6 and PTB7 pins cannot operate as open-drain pins. These pins actively drive high and low, similar to normal GPIO pins. As a result, when another device on the IIC bus drives low, there will be high current to this device when the corresponding pin of PTB6 and/or PTB7 drives high.

Workaround: Use the true open-drain PTA2 and PTA3 pins for the IIC SDA and SCL functions. Do not use PTB6 and PTB7 as IIC function pins. This issue will be fixed on future silicon revisions.

e7040: SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

Errata type: Errata

Description: Some devices may not start up as expected when both conditions are met: cold temperature (typically between -40°C and -10°C) and slow VDD ramp up time (typically between 500V/s to 900 V/s). The unstable startup is occasional and recoverable after an uncertain period of time. That is, some devices may start up after several hundreds of microseconds, while others may take several minutes to start up and the same device may start up as expected after several power cycles.

Workaround: Try to meet all the following conditions to reduce the possibility of this issue:

- Temperature above -10°C;
- VDD ramp up time: 13 V/s to 400 V/s, 1K V/s to 10K V/s

This erratum will be fixed in the next revision.

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