AK1599V

RF Transmitter for Satellite Communication

1. General Description

AK1599V is a RF transmitter integrating Quadrature Modulator, RF Amplifier, fractional / integer synthesizer and VCO which support RF output frequency from 1600MHz to 2200MHz. AK1599V achieves very low power consumption for Satellite Communication.

2. Feartures

Transmitter

- Integrated Local signal generator
- Integrated Quadrature Modulator
- Maximum output power: -13dBm minimum
- Integrated Gain control amplifier
- Gain range: 12dB typical

Supply Voltage/ Operating Temperature

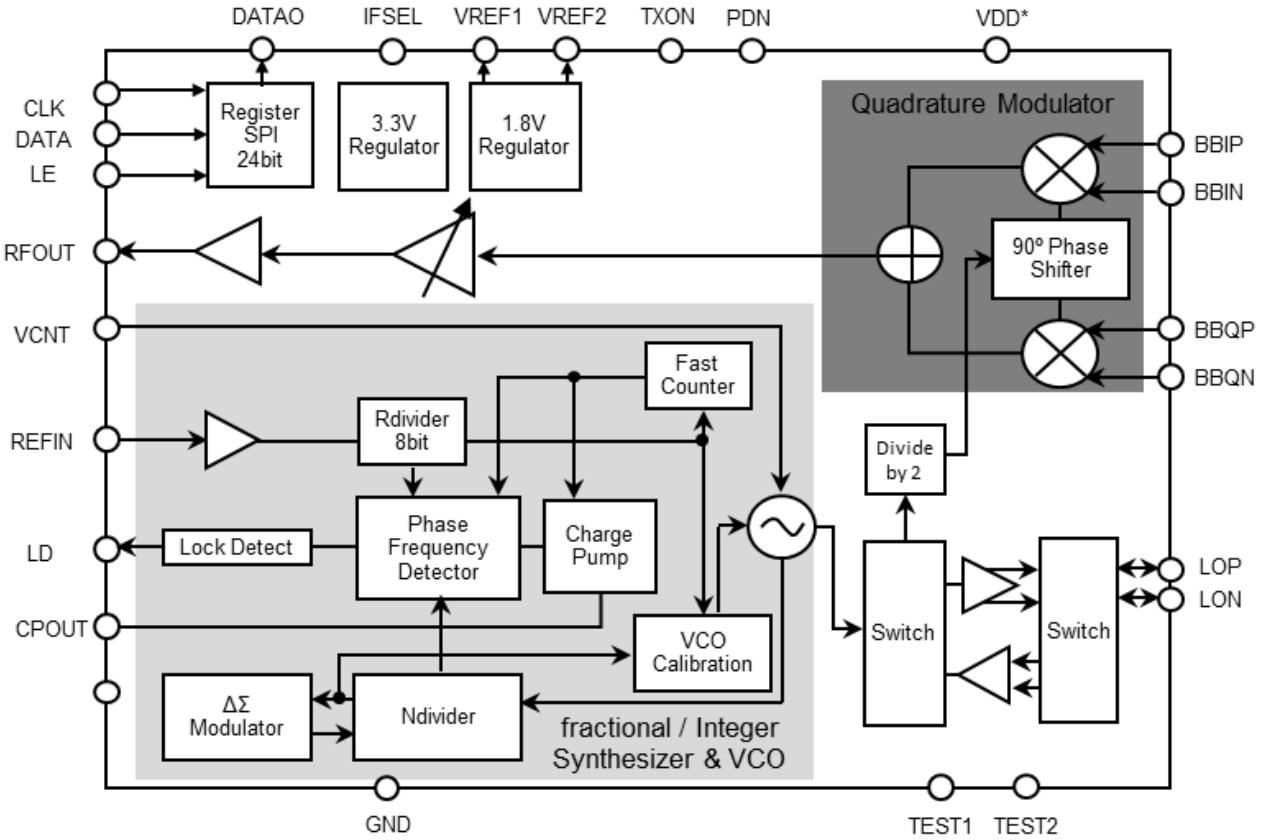
- Supply Voltage
  Analog: 5V
  Digital Interface: 5V / 3.3V (when internal 3.3V regulator is used)

- Operating Temperature -40 to 85 °C

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram



VDD*: CPBUFVDD, PVDD, MODVDD, MODVDD, BALVDD, TXVDD, LOVDD, OAVDD, SVDD, VCOVDD, CPVDD

Fig.1 Block Diagram

4.2. Functions

Table1. Block Functions

Block	Function
Quadrature Modulator	Up-convert baseband I/Q input signal to RF signal.
N divider	Frequency divider which divides the signal of VCO and pass it to phase frequency detector.
ΔΣ Modulator	Control the modulus of N divider and realize fractional dividing.
R divider	Frequency divider which divides the signal of reference clock and pass it to phase frequency detector.
Phase Frequency Detector (PFD)	Detect a phase difference between the divided VCO signal and comparison frequency, and then drive the charge pump.
Charge Pump	Output the electric charge according to the phase difference detected by PFD.
VCO	The voltage controlled oscillator.
1.8V Regulator	Create 1.8V for internal digital block.
3.3V Regulator	Create 3.3V for digital interface.

5. Pin Configurations and Functions

5.1. Pin Configurations

Top View

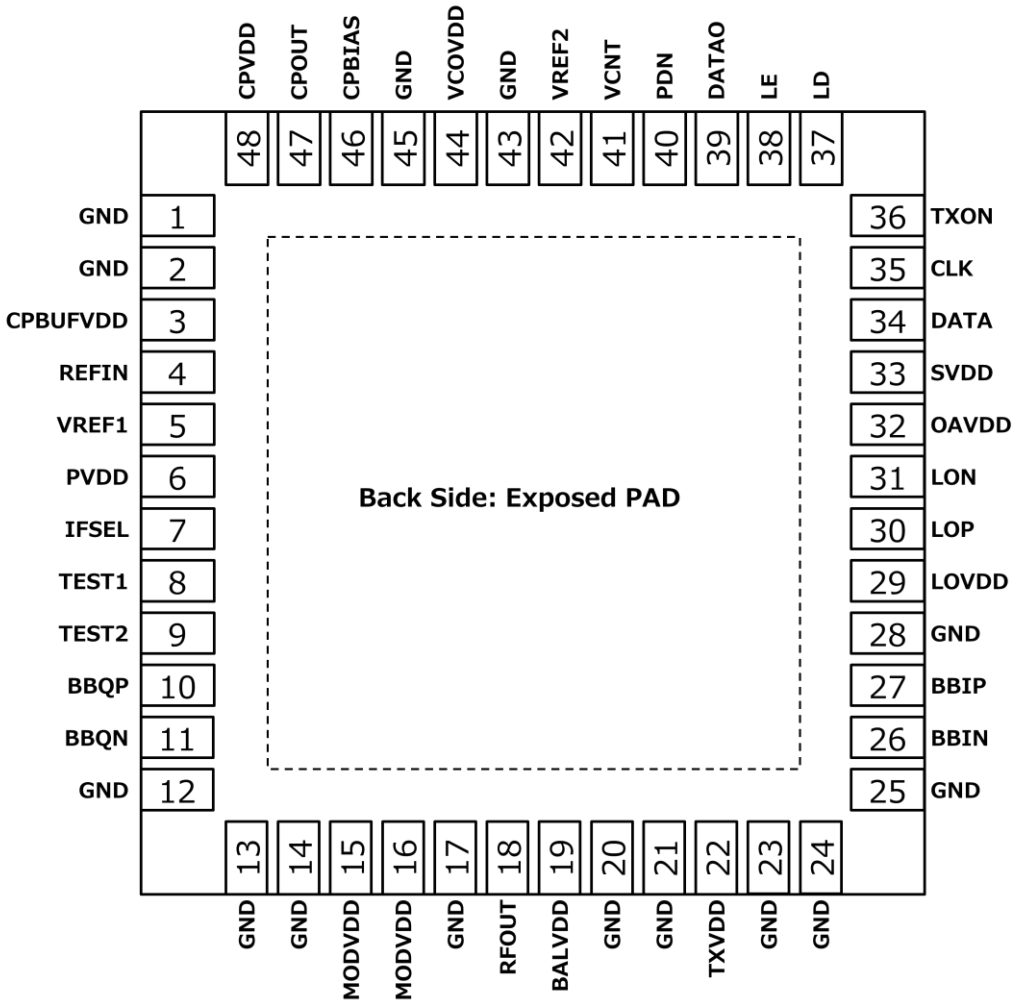


Fig.2 Pin Configuration

5.2. Functions

Table2. Pin Functions

Pin No.	Pin Name	I/O Type	Pin Description
1	GND	G	
2	GND	G	
3	CPBUFVDD	P	Charge Pump Pre-Buffer Power Supply.
4	REFIN	AI	Reference Input signal.
5	VREF1	AO	Connecting a capacitor and a resistor in series to the ground plane in order to stabilize internal 1.8V regulator for digital

Pin No.	Pin Name	I/O Type	Pin Description
			block.
6	PVDD	P	Synthesizer Power Supply.
7	IFSEL	DI	Enable/Disable internal 3.3V regulator for digital interface.
8	TEST1	DI	Connect to the ground plane.
9	TEST2	DI	Connect to the ground plane.
10	BBQP	AI	Baseband Differential Q Signal input.
11	BBQN	AI	Baseband Differential Q Signal input.
12	GND	G	
13	GND	G	
14	GND	G	
15	MODVDD	P	Quadrature Modulator Power Supply.
16	MODVDD	P	Quadrature Modulator Power Supply.
17	GND	G	
18	RFOUT	AO	RF signal output. Connecting matching network after a decoupling capacitor.
19	BALVDD	P	Balun Power Supply.
20	GND	G	
21	GND	G	
22	TXVDD	P	TX IREF Power Supply.
23	GND	G	
24	GND	G	
25	GND	G	
26	BBIN	AI	Baseband Differential I Signal input.
27	BBIP	AI	Baseband Differential I Signal input.
28	GND	G	
29	LOVDD	P	Local Power Supply.
30	LOP	AIO	Local differential Input / Output. Open this pin if not used.
31	LON	AIO	Local differential Input / Output. Open this pin if not used.
32	OAVDD	P	Local Output Amplifier Power Supply.
33	SVDD	P/AO	External Power Supply / Internal 3.3V regulator for digital interface (selected by IFSEL pin).
34	DATA	DI	Serial Data Input.
35	CLK	DI	Serial Clock Input.
36	TXON	DI	TX Power Control.
37	LD	DO	Lock Detection Output Interface.
38	LE	DI	Load Enable.
39	DATAO	DO	Output pin for read back data.
40	PDN	DI	Power Control. A logic low on this pin power down the device.
41	VCNT	AI	Control Input to VCO.
42	VREF2	AO	Connecting a capacitor to the ground plane in order to remove noise of internal 1.8V regulator for digital block.

Pin No.	Pin Name	I/O Type	Pin Description
43	GND	G	
44	VCOVDD	P	VCO Power Supply.
45	GND	G	
46	CPBIAS	AI	Connecting a resistor to the ground plane in order to create reference current for Charge Pump.
47	CPOUT	AO	Charge Pump Output.
48	CPVDD	P	Charge Pump Power Supply.

Exposed PAD on Back side of the package should be connected to GND

P : Power Supply G : Ground
AI : Analog Input AO : Analog Output AIO : Analog I/O
DI : Digital Input DO : Digital Output

6. Absolute Maximum Ratings

Table3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	VDD1	-0.3	5.5	V	Note1, Note2
	VDD2	-0.3	5.5	V	Note1, Note3
	VDD3	-0.3	5.5	V	Note1, Note4
GND Level	VSS	0	0	V	Voltage Reference Level, Note5
Maximum BB Input Level	BBPOW		10	dBm	Note6
Maximum Lo Input Level	LOPOW		12	dBm	Note7
Input Voltage	VAIN	VSS-0.3	VDD3+0.3	V	Note1, Note8
	VDIN1	VSS-0.3	VDD1+0.3	V	Note1, Note9
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	150	°C	
Maximum Junction Temperature	Tjmax		150	°C	

Note1 0V reference for all voltages
Note2 Applied to [SVDD] pin.
Note3 Applied to [BALVDD], [TXVDD], [MODVDD], [OAVDD] and [LOVDD] pins.
Note4 Applied to [CPVDD], [CPBUFVDD], [PVDD] and [VCOVDD] pins.
Note5 Applied to [GND] pin.
Note6 Applied to [BBIP], [BBIN], [BBQP] and [BBQN] pins.
Note7 Applied to [LOP] and [LON] pins.
Note8 Applied to [VCNT], [IFSEL] and [REFIN] pins.
Note9 Applied to [CLK], [DATA], [LE], [PDN] and [TXON] pins.

Table4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-pin QFN	26.7	18.1	°C/W

θ_{JA}: Thermal Resistance between junction and ambience
θ_{JC}: Thermal Resistance between junction and surface of package

Exceeding these maximum ratings may result in damage to AK1599V. Normal Operation is not guarantee at these extremes.

7. Recommended Operating Conditions

The specifications are applicable within operating range (supply voltage / operating temperature) specified below.

Table5. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Operating Temperature	-40		85	°C	
Supply Voltage					
VDD1	4.75	5	5.25	V	SVDD (Note1, Note2)
VDD2	4.75	5	5.25	V	TXVDD, BALVDD, MODVDD, LOVDD, OAVDD
VDD3	4.75	5	5.25	V	CPVDD, CPBUFVDD, PVDD, VCOVDD
VDD1 - VDD2	-0.1		0.1	V	(Note2)

Note1 This specification is applicable when SVDD is externally applied. Don't apply voltage to SVDD in internal 3.3V Regulator Mode.
Note2 VDD1 - VDD2 is the specification when SVDD is externally applied.

8. Electrical Characteristics

8.1. Analog Specification

Typical specifications: VDD1 = 5V, VDD2 = 5V, VDD3 = 5V, Baseband frequency 960 kHz
Baseband Continuous Wave (BBCW) Input = 0.5 (Vpp, differential). I/Q Input Bias Level = 0.5V
Operating Temperature = 25°C. Resistor connected to CPBIAS pin is 27kΩ.
Min/Max specifications are at "6.1 Recommended Operating Range". Operating Mode = State5. Unless otherwise noted.

Table6. Electrical Characteristics

Parameter		Min.	Typ.	Max.	Unit	Conditions
Power Consumption			1.3	1.7	W	PDN pin = TXON pin = "H", Ref = 40MHz, R divider = 1, PFD = 40MHz, DIV[1:0] bits = LOLV[1:0] bits = "00", Pomax(TXGAIN[6:0] bits = "1111111"), MODE[1:0] bits = "00"
RF Frequency Range		1600		2200	MHz	
Internal LO Frequency		1700		2100	MHz	
Internal VCO Frequency		3400		4200	MHz	
LO Input Level		-5		+5	dBm	
LOP / LON Return Loss			-10		dB	
LO Output Level			0 -2 -5 -11		dBm	LO = 3.8GHz LOLV[1:0] bits = "11" LOLV[1:0] bits = "10" LOLV[1:0] bits = "01" LOLV[1:0] bits = "00"
Transmitter						
RF Output Power		-13	-6		dBm	Pomax(TXGAIN[6:0] bits = "1111111") BB CW Input = 0.5(Vpp, differential)
RF Output Power over temperature			-0.5		dB	-40°C to 25°C or 25°C to 85°C
Output P1dB		0	4		dBm	Pomax(TXGAIN[6:0] bits = "1111111")
OIP3		10	14		dBm	Pomax(TXGAIN[6:0] bits = "1111111") (Baseband Frequency = 5MHz, 6MHz)
Spurs	Offset < 256kHz			-55	dBc	Pomax(TXGAIN[6:0] bits = "1111111") BB CW Input = 0.5(Vpp, differential) LO ≤ 1.9GHz, Only Integer Mode, Int ≤ 95, Frac = 0, Mod = 1, (Note1) Baseband Frequency < 100MHz Offset frequency is double side from carrier
	256kHz to 960kHz			-62	dBc	
	960kHz to 10MHz			-76	dBc	
	10MHz to 50MHz			-76	dBc	

Parameter	Min.	Typ.	Max.	Unit	Conditions
Carrier Suppression			-40	dBc	Pomax(TXGAIN[6:0] bits = ”1111111”) BB CW Input = 0.5(Vpp, differential)
Sideband Rejection			-40	dBc	Pomax(TXGAIN[6:0] bits = ”1111111”) BB CW Input = 0.5(Vpp, differential)
2nd Harmonics			-45	dBc	Pomax(TXGAIN[6:0] bits = ”1111111”) BB CW Input = 0.5(Vpp, differential) 2nd Harmonics(Pout - P(flo + 2fbb))
3rd Harmonics			-45	dBc	Pomax(TXGAIN[6:0] bits = ”1111111”) BB CW Input = 0.5(Vpp, differential) 3rd Harmonics(Pout - P(flo + 3fbb))
Output Return Loss		-15		dB	50Ω matched by recommended circuit shown on “11. Typical Evaluation Board Schematic”
Gain Control					
Gain Range		12		dB	
Gain Control Step		0.5		dB	
Base Band Inputs					
Input impedance		10		kΩ	IQ differential
Input Range			2	Vpp	IQ differential, Continuous Wave
1dB down BW		100		MHz	
I/Q Input Bias Level		0.5		V	
Power Down/Up Response Time		3	10	μs	Modulator and Amplifier can be ON/OFF by TXON pin. In case of Power Up, this is ±1dB settling time against final value. In case of Power down, this is the time before output power becomes under -60dBm.
PLL					
Integrated Phase Noise (Integer Mode)		0.18	0.23	degree rms	LO ≤ 1.9GHz, Only Integer Mode, 2.5 kHz to 4 MHz integration bandwidth Int ≤ 95, Frac = 0, Mod = 1, (Note1)
		0.21	0.25	degree rms	LO ≤ 2.1GHz, Only Integer Mode, 2.5 kHz to 4 MHz integration bandwidth Int ≤ 105, Frac = 0, Mod = 1, (Note1)
REFIN					
Input Sensitivity	0.7		2	Vpp	
Input Frequency	10		300	MHz	
PFD					
Phase Detector Frequency	1.2		40	MHz	

Parameter	Min.	Typ.	Max.	Unit	Conditions
Charge Pump					
Minimum Charge Pump Current		300		μA	
Maximum Charge Pump Current		2400		μA	
Icp TRI-STATE Leak Current		1		nA	Ta = 25°C
CP Output Range	0.5		VDD3 -0.5	V	
VCO					
Operating Frequency Range	3400		4200	MHz	VCO
VCO Phase Noise		-76		dBc/ Hz	10kHz offset, 3.6GHz
		-101		dBc/ Hz	100kHz offset, 3.6GHz
		-122		dBc/ Hz	1MHz offset, 3.6GHz
		-143		dBc/ Hz	10MHz offset, 3.6GHz
PLL switching time		1.7		ms	Jump from unlocked state to LO = 1.9GHz ±2.5Hz settling time, (Note1)
		1.4	2.2	ms	Jump from 1.7G to 2.1GHz, 2.1G to 1.7GHz ±2.5Hz settling time, (Note1)
IDD					
IDD1		2		mA	PDN pin = “L”
IDD2		260	324	mA	PDN pin = TXON pin = “H”, Ref = 40MHz, R divider = 1, PFD = 40MHz, DIV[1:0] bits = LOLV[1:0] bits = “00”, Pomax(TXGAIN[6:0] bits = ”1111111”), MODE[1:0] bits = “00”
IDD3		280		mA	PDN pin = TXON pin = “H”, Ref = 40MHz, R divider = 1, PFD = 40MHz, DIV[1:0] bits = LOLV[1:0] bits = “00”, Pomax(TXGAIN[6:0] bits = ”1111111”), MODE[1:0] bits = “01”

Note1 Ref = 40MHz, PFD = 40MHz, R divider = 1
Loop Filter: C1 = 100pF, C2 = 8.2nF, C3 = 100pF, R2 = 1.2kΩ, R3 = 1kΩ, CP1 = 900μA

8.2. Digital Specification

Table7. Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
High Level Input Voltage	Vih1		0.8×VDD1			V	Note1
	Vih2		0.8×VDD3			V	Note2
	Vih3	Note4	2.4			V	Note1
Low Level Input Voltage	Vil1				0.2×VDD1	V	Note1
	Vil2				0.2×VDD3	V	Note2
	Vil3	Note4			0.6	V	Note1
High Level Input Current	Iih1	Vih=VDD1=5.25V	-1		1	μA	Note1
	Iih2	Vih=VDD3=5.25V	-1		1	μA	Note2
Low Level Input Current	Iil1	Vil=0V, VDD1=5.25V	-1		1	μA	Note1
	Iil2	Vil=0V, VDD3=5.25V	-1		1	μA	Note2
High Level Output Voltage	Voh1	Ioh = -500μA	VDD1-0.4			V	Note3
	Voh2	Note4 Ioh = -500μA	2.8			V	Note3
Low Level Output Voltage	Vol	Iol = 500μA			0.4	V	Note3

Note1 Applied to [CLK], [DATA], [LE], [PDN] and [TXON] pins.
Note2 Applied to [IFSEL] pin.
Note3 Applied to [LD] and [DATAO] pins.
Note4 Internal 3.3V Regulator Mode

2. Serial Interface Timing

<Write-In Timing>

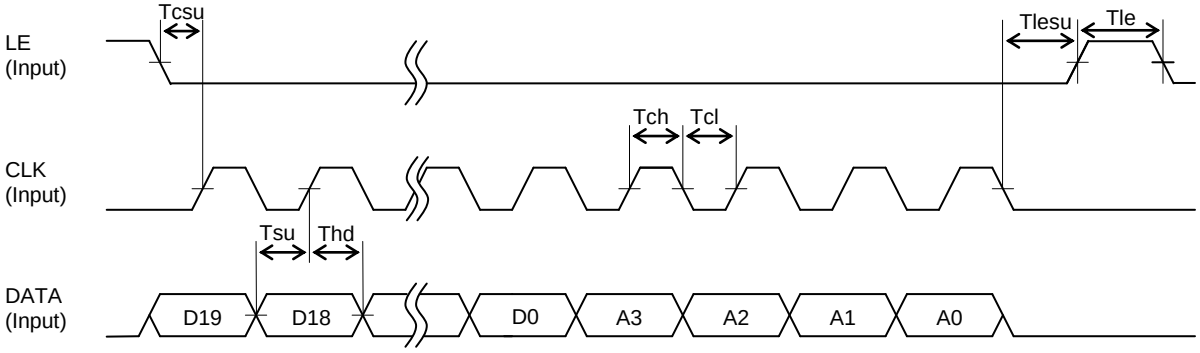


Fig.3 Serial Interface Timing (Write-In)

<Read-Back Timing>

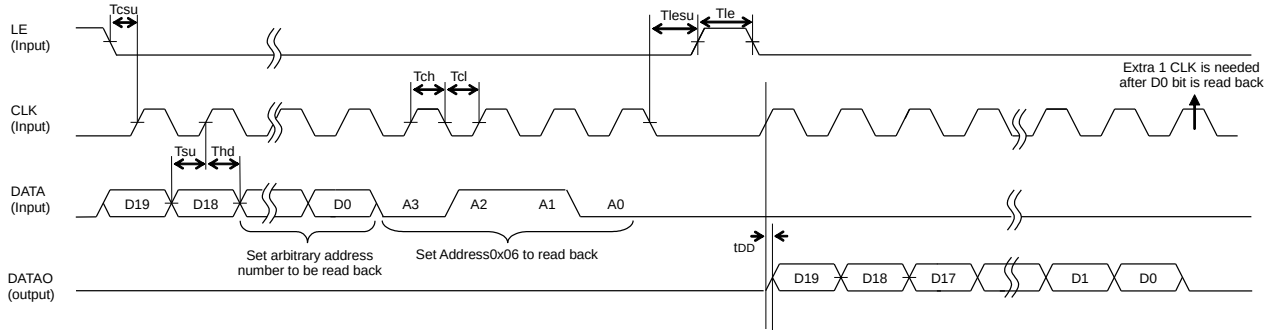


Fig.4 Serial Interface Timing (Read-Back)

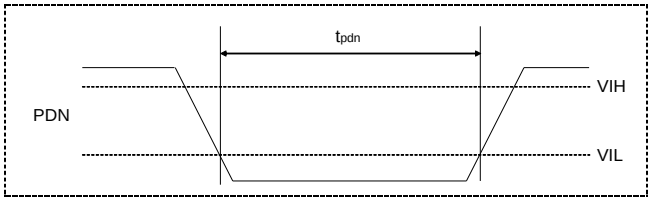


Fig.5 Power Down Pin Timing

Table8. Digital AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock L level hold time	Tcl		25			ns	
Clock H level hold time	Tch		25			ns	
Clock setup time	Tcsu		10			ns	
Data setup time	Tsu		10			ns	
Data hold time	Thd		10			ns	
LE setup time	Tlesu		10			ns	
LE pulse width	Tle		25			ns	
CLK to DATAO output delay time	tDD	15pF Load			20	ns	
PDN pin “L” level hold time	tpdn		1			μs	

Be sure to input CLK when LE pin = “L” otherwise AK1599V is going to malfunction.

9. Functional Descriptions

9.1. Operating Mode

(a) Operating mode controlled by PDN pin, TXON pin and MODE[1:0] bits

Table9. Operating Mode

Mode	Pin	Pin	Registers		Operation of each block			
	PDN	TXON	MODE [1]	MODE [0]	TX Block	Synthesizer Block	VCO Block	LOP, LON pin
State 0	0	X	X	X	OFF	OFF	OFF	OFF
State 1	1	0	0	0	OFF	ON	ON	OFF
State 2	1	0	0	1	OFF	ON	ON	Output
State 3	1	0	1	0	OFF	ON	OFF	Input
State 4	1	0	1	1	OFF	OFF	OFF	Input
State 5	1	1	0	0	ON	ON	ON	OFF
State 6	1	1	0	1	ON	ON	ON	Output
State 7	1	1	1	0	ON	ON	OFF	Input
State 8	1	1	1	1	ON	OFF	OFF	Input

State0: Standby mode. Current Consumption becomes minimum. Register setting is available. (Note)
State1: VCO and Synthesizer operate.
State2: VCO and Synthesizer operate and output its signal from LOP, LON pins.
State3: Only Synthesizer operates. PLL can be operated by using external VCO.
State4: Standby mode. Current Consumption becomes minimum. Register setting is available. (Note)
State5: TX block operates in addition to State1.
State6: TX block operates in addition to State2.
State7: TX block operates in addition to State3.
State8: TX block operates. Input local signal from LOP, LON pins.

(Note) After powering on AK1599V, the initial registers values are not defined. It is required to write the data in all addresses.

(b) Digital interface voltage option selected by IFSEL pin

Regarding SVDD which is power supply for digital interface, either external power supply (5V) or internal 3.3V regulator can be selected.

Table10. Function of IFSEL pin

IFSEL	SVDD
“L” (should be connected to GND)	External Power Supply (5V)
“H” (should be connected to PVDD)	Internal 3.3V regulator

9.2. PLL

The Phase Locked Loop consists of a Fractional / Integer Frequency synthesizer. The PLL covers LO frequency range from 1700MHz to 2100MHz. It also has an integrated voltage controlled oscillator (VCO) which achieves good phase noise performance.

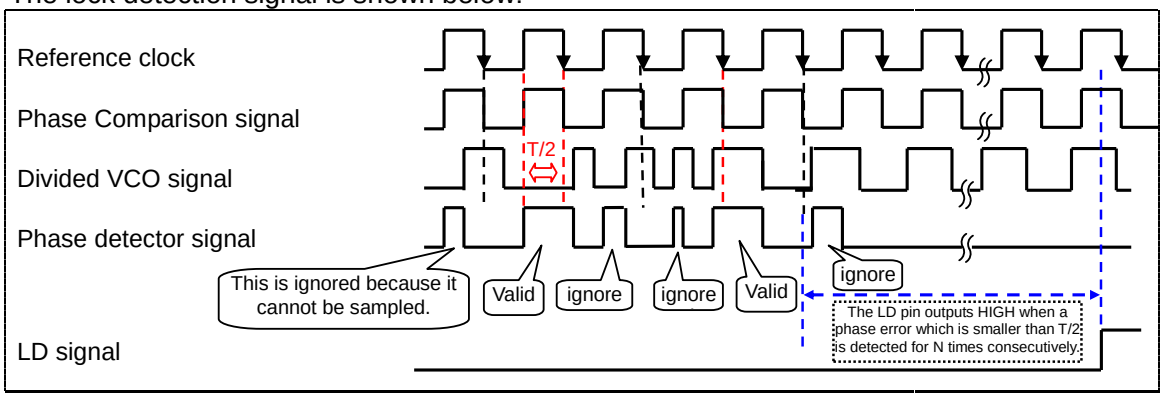
9.3. Lock Detection

Lock detection output can be selected by LD bit in Address0x04. When LD bit = “1”, LD pin outputs a phase comparison result which is from phase detector directly (This is called “analog lock detection”). When LD bit = “0”, the output is the lock detection signal according to the on-chip logic (This is called “digital lock detection”).
The digital lock detection can be done as following:
LD pin stays unlocked state (which outputs “L”) when frequency setup is made.
In the digital lock detection, LD pin signal rises to “H” (which means the locked state) after a phase error smaller than a cycle of [REFIN] clock (T) is detected for N times consecutively. After a phase error larger than T is detected for N times consecutively when LD pin = “H”, LD pin signal drops to “L” (which means the unlocked state). The counter value N can be set by LDCNTSEL bit in Address0x04. The N is different between “unlocked to locked” and “locked to unlocked”.

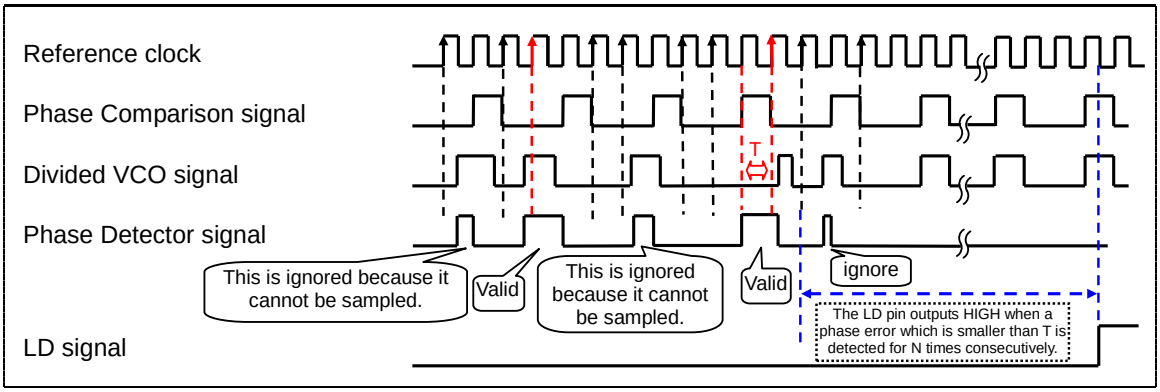
Table11. Lock Detection Precision

LDCNTSEL bit	unlocked to locked	locked to unlocked
“0”	N = 15	N = 3
“1”	N = 31	N = 7

The lock detection signal is shown below:



Case of “R = 1” (Note)



Case of “R > 1” (Note)

(Note) R is registers in Address0x03

Fig.6 Digital Lock Detection Operations

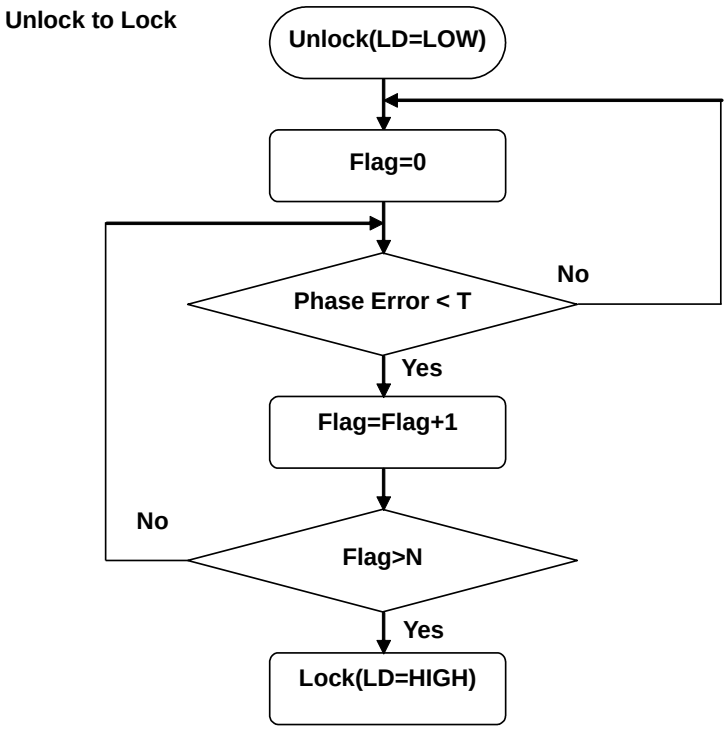


Fig.7 Unlock to Lock

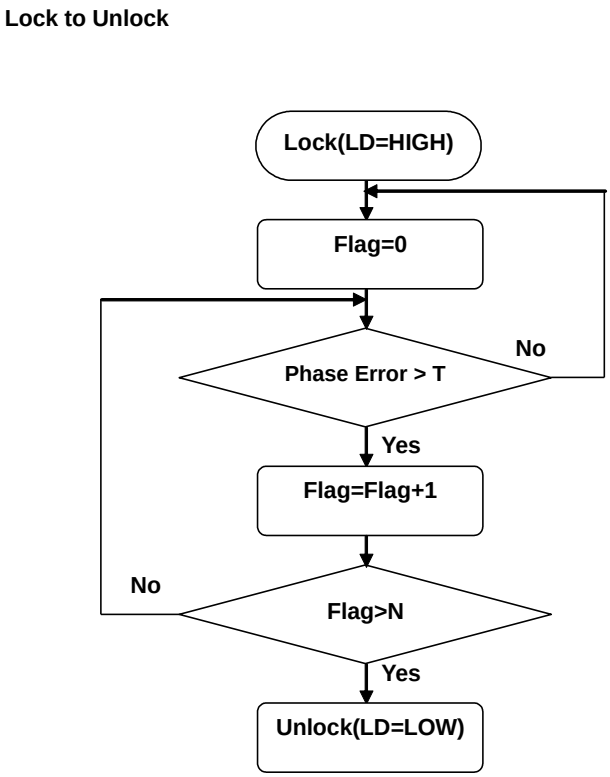


Fig.8 Lock to Unlock

9.4. Frequency Settings

<Synthesizer settings>

The following formula is used to calculate the frequency setting for the AK1599V.

Setting Frequency = Ref Frequency * (INT + FRAC / MOD)	
Ref Frequency	: Phase detector frequency
INT	: Setting value of Integral divider (Refer to Address0x01: INT[11:0] bits)
FRAC	: Setting value of numerator (Refer to Address0x02: FRAC[11:0] bits)
MOD	: Setting value of denominator (Refer to Address0x03: MOD[11:0] bits)

Set INT[11:0] bits within a range from 35 to 4091.
Set FRAC[11:0] bits in accordance with following range : 0 ≤ FRAC ≤ (MOD-1).
Set MOD[11:0] bits within a range from 2 to 4095.

○ Calculation example

In order to achieve setting frequency = 3602MHz with Ref Frequency = 40MHz, set following values.
RFOUT Carrier frequency is the half of synthesizer setting frequency.

INT	=	90
FRAC	=	1
MOD	=	20

Synthesizer setting Frequency = 40MHz * (90 + 1 / 20) = 3602MHz
RFOUT carrier frequency = 3602MHz / 2 = 1801MHz

Frequency Settings are done by setting Address0x01, 0x02 and 0x03. The settings of Address0x02 and 0x03 are reflected simultaneously with setting Address0x01. Synthesizer block should be powered on before Address0x01 is set. Frequency settings, VCO calibration and Fast Lock Counter start its operation simultaneously with setting Address0x01. In order to set frequency correctly, be sure to set Address0x01 after setting PDN pin = ”H” and MODE[1:0] bits in Address 0x04 = “00” or “01”.

9.5. Fast lock up mode

The fast lock up mode becomes effective by setting FASTEN bit of address 0x04 = ”1”.
○Fast lock up mode
After setting Address0x01 when FASTEN bit = “1”, Fast Lock Up mode starts after VCO calibration. The Fast Lock Up mode is enabled only when the time period set by the timer according to the counter value defined by FAST [3:0] bits in Address0x04. The charge pump current is set to the value specified by CP2 bit. After the specified time period elapses, the Fast Lock Up mode is finished and switched to the normal operation, and the charge pump current returns to CP1 bit setting.

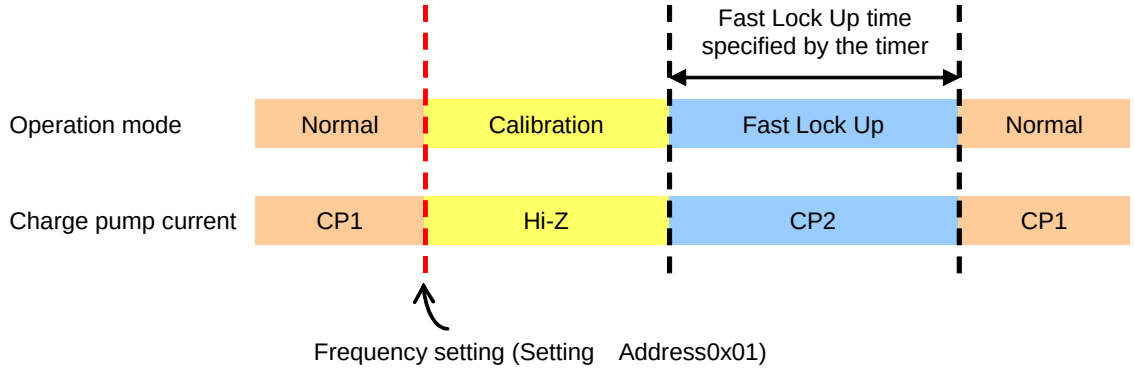


Fig.9 Fast Lock up Mode Timing Chart

○**Timer period**
FAST[3:0] bits in Address0x04 is used to set the time period for the fast lock mode. The following formula is used to calculate the time period

Time period = (511 + FAST[3:0] × 512) / PFD frequency

9.6. VCO

<Calibration>

The calibration starts by setting Address0x01 when MODE[1:0] bits in Address 0x04 = “00” or “01” and PDN pin = ”H”. During the calibration, VCO VTUNE is disconnected from the output of the loop filter and connected to an internal reference voltage. In addition, the charge pump output is disabled during calibration.
The internal reference voltage must be stable so that the calibration is done correctly. Therefore, after setting PDN pin = “H”, it is necessary to wait 500μs at least before setting Address0x01.
CALTM[3:0] bits determines the calibration time. The larger CALTM[3:0] bits are set, the higher calibration precision becomes, but the calibration time becomes long. The value calculated by the following formula is recommended to achieve enough calibration precision. However, CALTM[3:0] bits should be set between 1 and 11. 0 and over 12 are prohibited.

CALTM[3:0] ≥ log2 (PFD frequency / 20000)

The calibration time can be estimated as following calculation.

Calibration time = 1 / PFD frequency × {(6 + 2 ^ {CALTM [3:0]}) × 8 + 3}

9.7. Loop Filter

Fig. 10 shows loop filter topology used to evaluate AK1599V.

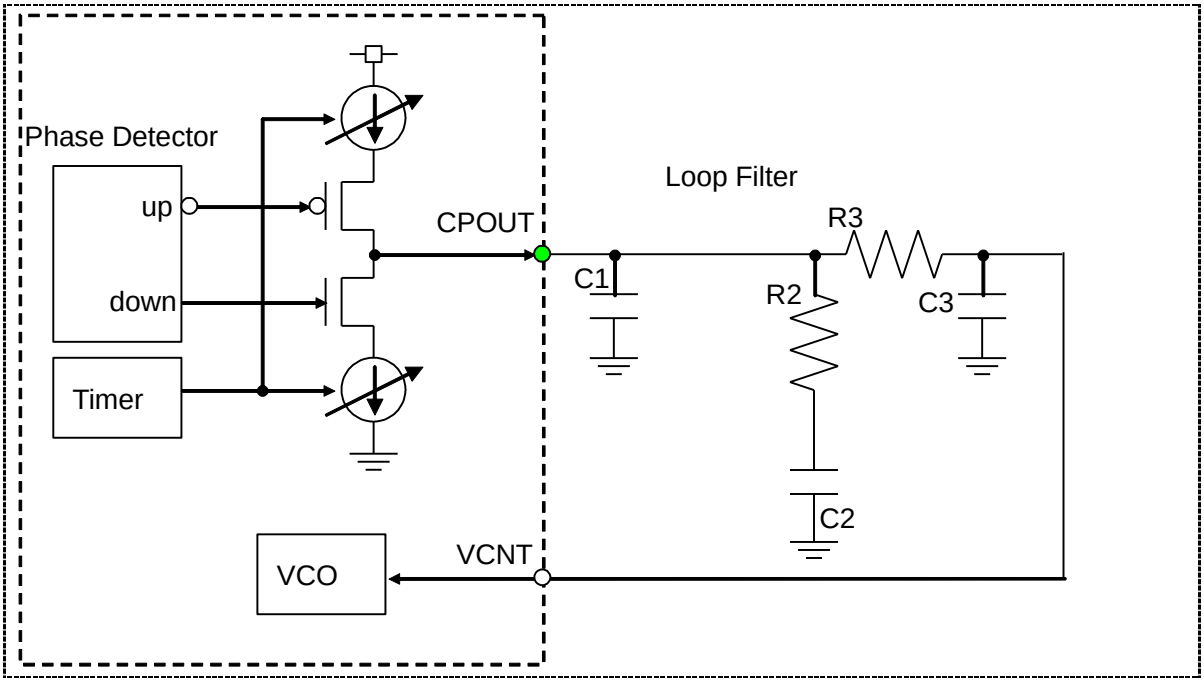
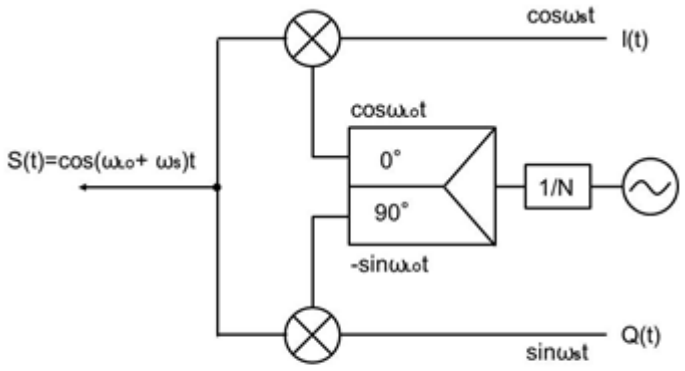


Fig.10 Loop Filter

9.8. Quadrature Modulator

AK1599V consists of Quadrature Modulator, RF amplifier, and Programmable attenuator. A polarity of Quadrature Modulator is as follows. Recommended DC bias Voltage to Baseband I/Q Input is 0.5V±0.025V.



I (t) : A differential input of IIP and IIN
Q(t) : A differential input of IQP and IQN
S(t) : RF Output

Fig.11 Block diagram of internal Quadrature Modulator

9.9. SPI & Register

AK1599V contains Serial Peripheral Interface (SPI) which provides write and read access to internal registers that are used to configure the device.

10. Register Map

Register Settings

Name	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
Freq1				VCO [1]	VCO [0]	DIV [1]	DIV [0]		INT [11]	INT [10]	INT [9]	INT [8]	INT [7]	INT [6]	INT [5]	INT [4]	INT [3]	INT [2]	INT [1]	INT [0]	0x01
Freq2		CP1 [2]	CP1 [1]	CP1 [0]		CP2 [2]	CP2 [1]	CP2 [0]	FRAC [11]	FRAC [10]	FRAC [9]	FRAC [8]	FRAC [7]	FRAC [6]	FRAC [5]	FRAC [4]	FRAC [3]	FRAC [2]	FRAC [1]	FRAC [0]	0x02
Freq3	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	MOD [11]	MOD [10]	MOD [9]	MOD [8]	MOD [7]	MOD [6]	MOD [5]	MOD [4]	MOD [3]	MOD [2]	MOD [1]	MOD [0]	0x03
Function1	CAL TM [3]	CAL TM [2]	CAL TM [1]	CAL TM [0]		LD CNT SEL	LD	MTLD	FAST EN	FAST [3]	FAST [2]	FAST [1]	FAST [0]	CP HIZ	CP POLA		MO DE [1]	MO DE [0]	LOLV [1]	LOLV [0]	0x04
Function2														TXGA IN[6]	TXGA IN[5]	TXGA IN[4]	TXGA IN[3]	TXGA IN[2]	TXGA IN[1]	TXGA IN[0]	0x05
Read Back															READ DAD D[5]	READ DAD D[4]	READ DAD D[3]	READ DAD D[2]	READ DAD D[1]	READ DAD D[0]	0x06
INITIAL1															INITI AL1 [5]	INITI AL1 [4]	INITI AL1 [3]	INITI AL1 [2]	INITI AL1 [1]	INITI AL1 [0]	0x07
INITIAL2																			INITI AL2 [1]	INITI AL2 [0]	0x0D

Note of writing into registers

1. The settings of Address0x02 and 0x03 are reflected to internal circuits simultaneously with setting Address0x01.
2. It is possible to set Address0x04, 0x05, 0x06, 0x07 and 0x0D separately.
3. After powering up AK1599V, the initial registers value is not defined. It is required to write the data in all addresses.

< Address0x01: Freq1 >

D[16:15]

VCO[1:0]: Set VCO

Write “2” to VCO[1:0] to set VCO.

VCO[1:0]	VCO oscillating frequency
0	Prohibited
1	Prohibited
2	3.1GHz to 4.4GHZ
3	3.1GHz to 4.4GHZ

D[14:13]

DIV[1:0]: Local Divider

Write “0” to DIV[1:0] to set Local Divider.

DIV[1:0]	Division Ratio
0	2 divide
1	2 divide
2	Prohibited
3	Prohibited

D[11:0]

INT[11:0]: N divider

Set the number integral part of divide for synthesizer.
The allowed range is from 35 to 4091.

INT[11:0]	Division Ratio
0	Prohibited
1	Prohibited
-	-
34	Prohibited
35	35
36	36
-	-
-	-
4089	4089
4090	4090
4091	4091
4092	Prohibited
4093	Prohibited
4094	Prohibited
4095	Prohibited

< Address0x02: Freq2 >

D[18:16]

CP1[2:0]: Settings of the charge pump current for normal mode

D[14:12]

CP2[2:0]: Settings of the charge pump current for fast lock up mode

It is possible to set two types of charge pump current, CP1 and CP2.
CP1 is the charge pump current setting for the normal mode.
CP2 is the charge pump current setting for the fast lock up mode.
Charge pump current is as follows.

CP1[2:0], CP2[2:0]	Charge pump current [typ. μA]
0	300
1	600
2	900
3	1200
4	1500
5	1800
6	2100
7	2400

R = 27kΩ
R: Resistor value which is connected to CPBIAS pin

D[11:0]

FRAC[11:0]: Fractional Numerator determination
Set the Numerator of Fractional divider.
The allowed range is from 0 to MOD[11:0].
When FRAC is set to 0, ΔΣ modulator is inactivated and synthesizer operates as Integer-N synthesizer.

< Address0x03: Freq3 >

D[19:12]

R[7:0]: 8bit Reference divider

Maximum PFD frequency is 40MHz.

R[7:0]	Division Ratio
0	Prohibited
1	1
2	2
3	3
4	4
-	-
-	-
-	-
253	253
254	254
255	255

D[11:0]

MOD[11:0]: Fractional Denominator determination

Set the denominator of Fractional divider.
The allowed range is from 2 to 4095.

MOD[11:0]	Division Ratio
0	Prohibited
1	Prohibited
2	2
3	3
-	-
-	-
4089	4089
4090	4090
4091	4091
4092	4092
4093	4093
4094	4094
4095	4095

< Address0x04: function1 >

D[19:16]
CALTM[3:0]: Set the calibration precision of VCO
CALTM[3:0] bits determines the calibration precision of VCO and time. The larger CALTM[3:0] bits are set, the higher calibration precision becomes, but the calibration time becomes long as trade-off. The value calculated by the following formula is recommended to achieve enough calibration precision. However, CALTM[3:0] bits should be set between 1 and 11. 0 and Over 12 are prohibited.

$$CALTM[3:0] \geq \log_2 (PFD\ frequency / 20000)$$

The calibration time can be estimated as following calculation;

$$Calibration\ time = 1 / PFD\ frequency \times \{(6 + 2\ ^\wedge\ \{CALTM[3:0]\}) \times 8 + 3\}$$

D[14]

LDCNTSEL: Lock Detection Precision
Set the counter value for digital lock detection.

LDCNTSEL	Function	
0	15 times Count	unlocked to locked
	3 times Count	locked to unlocked
1	31 times Count	unlocked to locked
	7 times Count	locked to unlocked

D[13]

LD: Lock detection function
Set the lock detection function. Refer to "8.2.1.Lock Detection" for details.
0: Digital lock detection
1: Analog lock detection

D[12]

MTLD: Local signal mute. Select disable or enable to mute during unlocked state.

0: Disable to mute local signal during unlocked state
1: Enable to mute local signal during unlocked state

Be sure to set MTLD bit = 0 when LD bit = 1, so that Lock detection is Analog mode.

D[11]

FASTEN: Fast lock up mode setting
Set enable / disable fast lock up mode.
0: Disable fast lock up mode
1: Enable fast lock up mode
Refer to "8.2.3. Fast lock up mode" for details.

D[10:7]

FAST[3:0]: Fast lock timer setting
Set the count number of fast lock timer.
Count Number = 511+ FAST[3:0] × 512

FAST[3:0]	Count Number
0	511
1	1023
2	1535
3	2047
4	2559
5	3071
6	3583
7	4095
8	4607
9	5119
10	5631
11	6143
12	6655
13	7167
14	7679
15	8191

D[6]

CPHIZ: Charge Pump Hi-Z
Set the charge pump state to Hi-Z.
0: Normal
1: Hi-Z (Prohibited)

Be sure to set CPHIZ bit = “0”.

D[5]

CPPOLA: Charge pump output polarity
Set the charge pump output polarity.
0: Negative (Prohibited)
1: Positive

Be sure to set CPPOLA bit = “1”.

D[3:2]

MODE[1:0]: Local operation mode
Set the operation of Synthesizer, VCO, LOP and LON pins.

MODE[1:0]	Local Operating MODE
0	Internal Synthesizer and VCO are activated.
1	Internal Synthesizer and VCO are activated and the local signal is output from LOP and LON pins.
2	Internal VCO is inactivated. External VCO can be used with internal synthesizer.
3	Internal Synthesizer and VCO are inactivated. External local signal can be used.

Synthesizer setting frequency is output from LOP and LON pins when MODE[1:0] bits = “1”.
Refer to “8.2.2 Frequency Settings” for details.
The double carrier frequency of RFOUT should be input from LOP and LON pins when MODE[1:0] bits = “3”.

D[1:0]

LOLV[1:0]: Local output Power

When MODE[1:0] bits = “1”, set the power of the local signal output from LOP and LON pins.

LOLV[1:0]	LOP, LON output power [dBm]
0	-11
1	-5
2	-2
3	0

< Address0x05: function2 >

D[6:0]

TXGAIN[6:0]: Switching attenuator gain of TX block.

It is possible to set gain by 0.5dB step.

TXGAIN[6:0]	Attenuation [dB]
1111111	0
1111110	-0.5
1111101	-1
1111100	-1.5
:	:
1101000	-11.5
1100111	-12
1100110	Prohibited
:	:
0000000	Prohibited

< Address0x06: Read Back >

D[5:0]

READADD[5:0]: Read Back

Set address of register whose data will be read back and output from DATAO pin.
Regarding the output timing, refer to” 7.3 Digital Specification”.
Set following address and data whenever read back is done.

<Address0x0D: INITIAL2> 00000h

< Address0x07: INITIAL1 >

D[5:0] INITIAL1[5:0]: This register must be set right after power-up

< Address0x0D: INITIAL2 >

D[1:0] INITIAL2[1:0]: This register must be set right after power-up

11. Power up Sequence

■ Recommended Power up Sequence

PDN pin resets digital block except registers and powers down analog block. On the other hand, AKM recommends user to set all registers before powering up analog block because registers don't have reset. LOP/LON don't output any undesired signal in the recommended power up sequence. However, DATAO pin may output undesired signal for a period of 20CLK from CLK starts because initial value of Flip-Flop for ReadBack is undefined. RFOUT pin doesn't output undesired signal by setting TXON pin = "L".

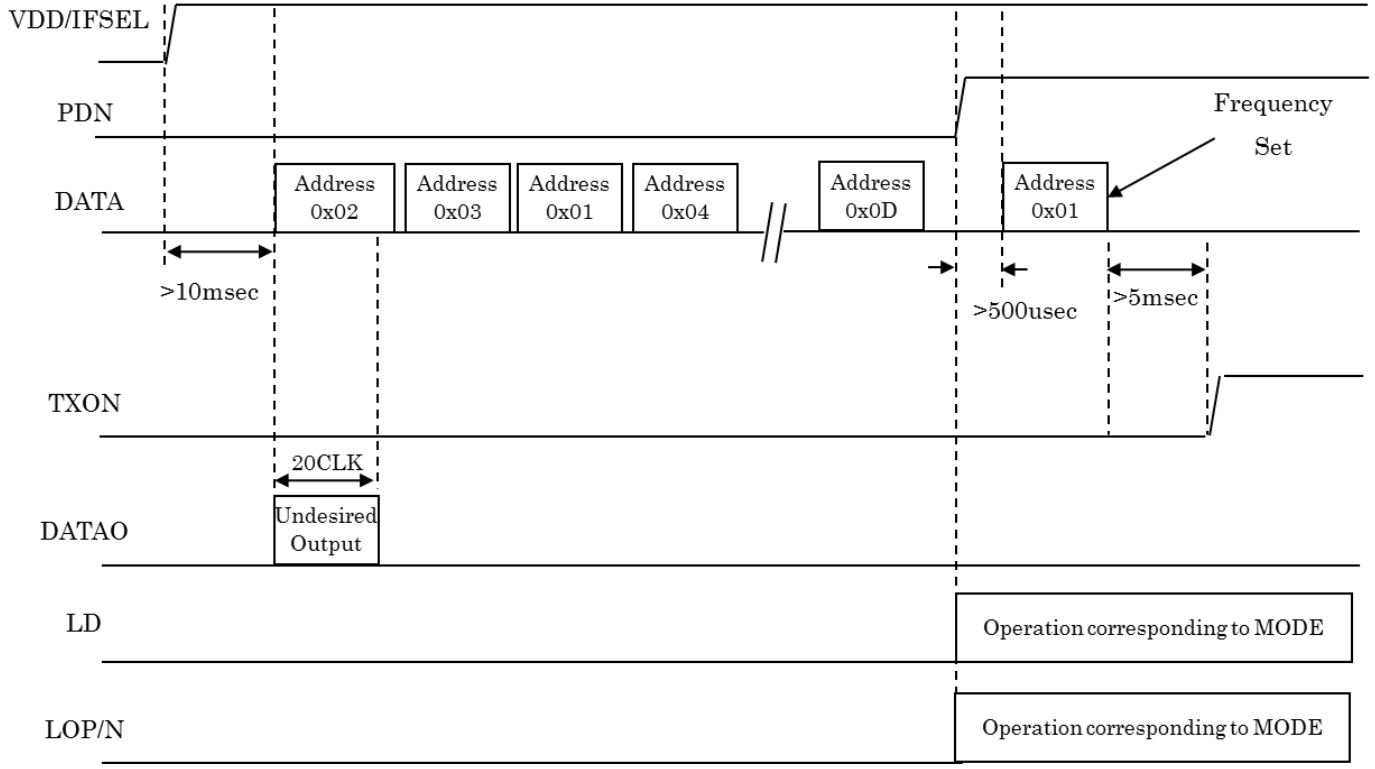


Fig.12 Recommended Power up Sequence (Internal 3.3V Regulator Mode)

Power up Sequence should be done as follows.

[1] Power up VDD/IFSEL
[2] 10ms after VDD is powered up, set all registers as following order. (Note1)

<Address0x02:Freq2> Arbitrary Data
<Address0x03:Freq3> Arbitrary Data
<Address0x01:Freq1> Arbitrary Data
<Address0x04:Function1> Arbitrary Data
<Address0x05:Function2> Arbitrary Data
<Address0x07:INITIAL1> 00001h
<Address0x0D:INITIAL2> 00000h
<Address0x0D:INITIAL2> 00003h
<Address0x0D:INITIAL2> 00000h

[3] Power up PDN
[4] 500μs after PDN is powered up, set the register as follows. (Note2)

<Address0x01:Freq1> Arbitrary Data

[5] 5ms after Address0x01 is set, power up TXON. (Note3)

(Note1) 10ms is waiting time for internal regulator to become stable
(Note2) 500μs is waiting time for synthesizer analog block to start up and become stable
(Note3) 5ms is waiting time for local frequency to become stable

■ Power up Sequence of VDD/IFSEL and PDN pin simultaneous launch (Internal 3.3V Regulator Mode)

PDN pin resets digital block except registers and powers down analog block. First of the sequence, be sure to power down analog block by setting MODE[1:0] in Address0x04 = ”11”. LOP, LON and LD pins may output undesired signal before setting MODE[1:0] = ”11” because initial value of registers is undefined. DATAO pin may output undesired signal for a period of 20CLK from CLK starts. RFOUT pin doesn’t output undesired signal by setting TXON pin = “L”.

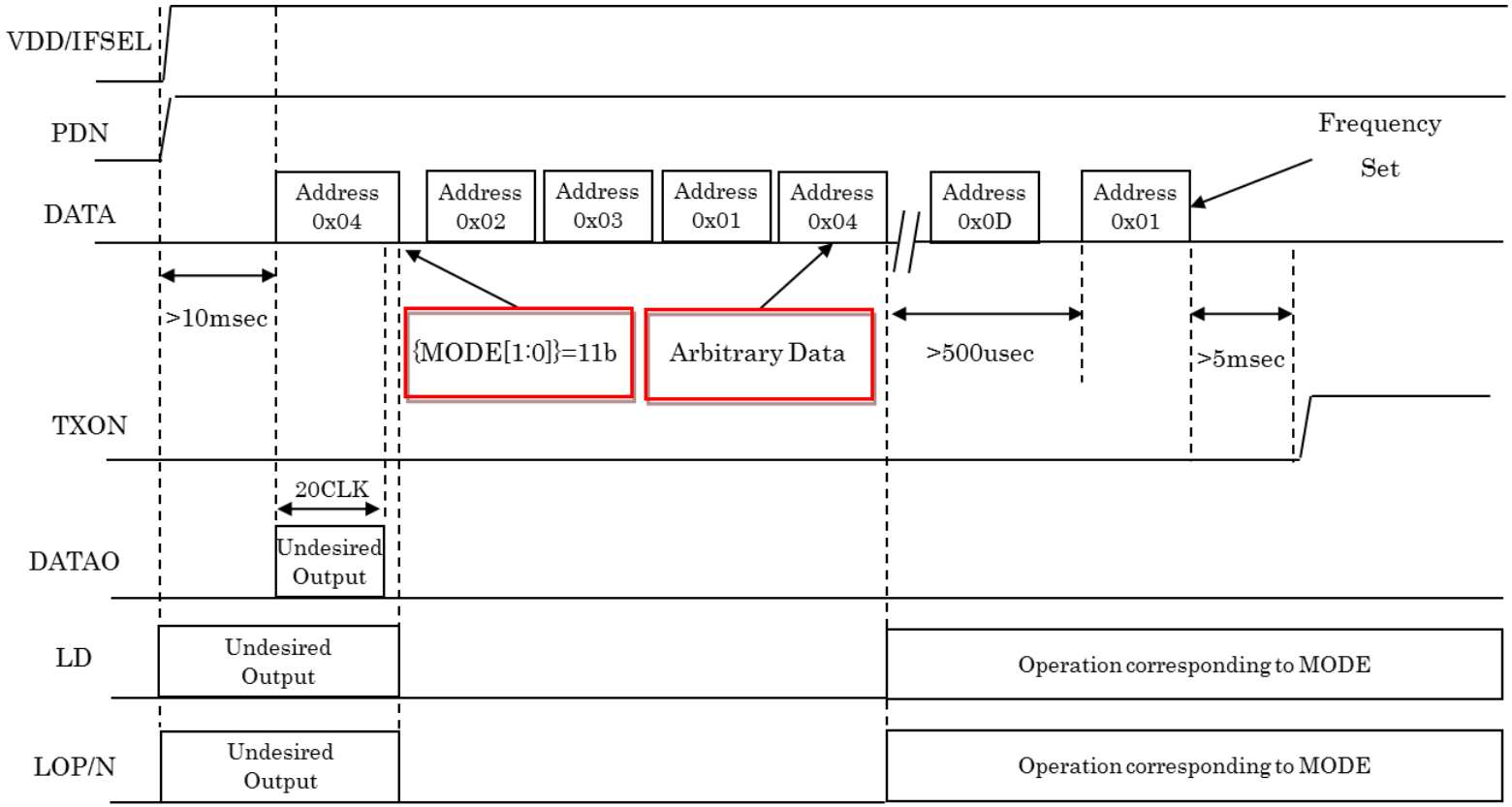


Fig.13 Power up Sequence of VDD/IFSEL and PDN pin simultaneous launch (Internal 3.3V Regulator Mode)

Power up Sequence of VDD / IFSEL and PDN pin simultaneous launch should be done as follows.

[1] Power up VDD / IFSEL and PDN
[2] 10ms after VDD is powered up, set all registers as following order. (Note4)

<Address0x04:Function1> MODE [1:0] = 11b, the other data is arbitrary
<Address0x02:Freq2> Arbitrary Data
<Address0x03:Freq3> Arbitrary Data
<Address0x01:Freq1> Arbitrary Data
<Address0x04:Function1> Arbitrary Data
<Address0x05:Function2> Arbitrary Data
<Address0x07:INITIAL1> 00001h
<Address0x0D:INITIAL2> 00000h
<Address0x0D:INITIAL2> 00003h
<Address0x0D:INITIAL2> 00000h

Wait for 500μs after "<Address0x04:Function1> Arbitrary Data" is set (Note5)

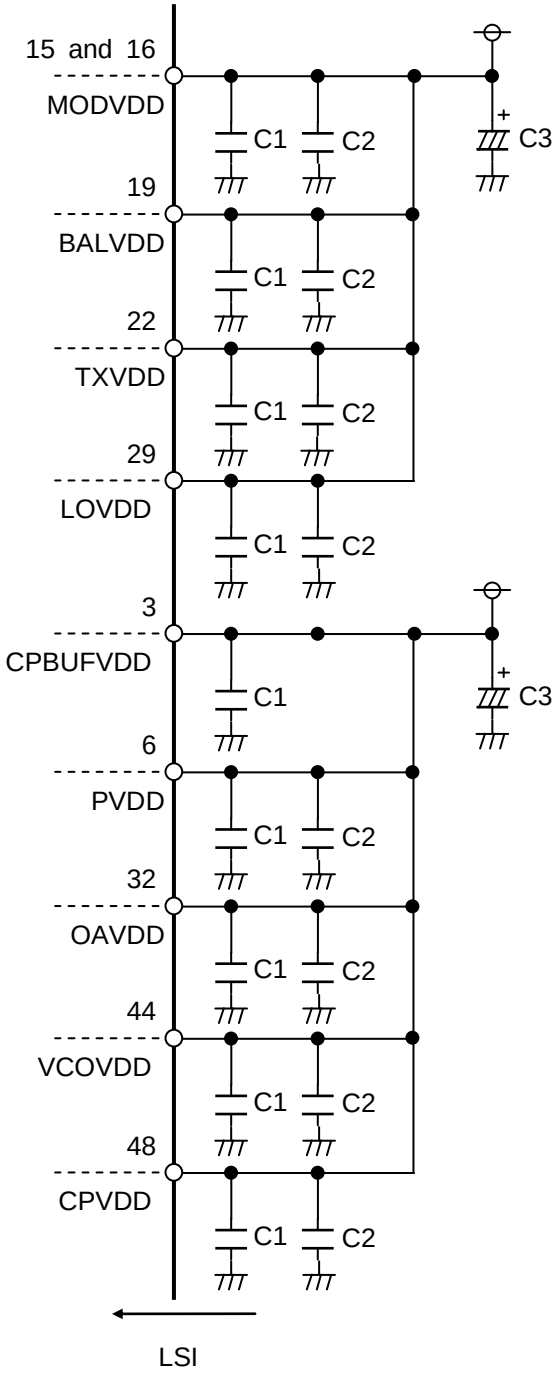
<Address0x01:Freq1> Arbitrary Data

[3] 5ms after Address0x01 is set, power up TXON. (Note6)

(Note4) 10ms is waiting time for internal regulator to become stable
(Note5) 500μs is waiting time for synthesizer analog block to start up and become stable
(Note6) 5ms is waiting time for local frequency to become stable

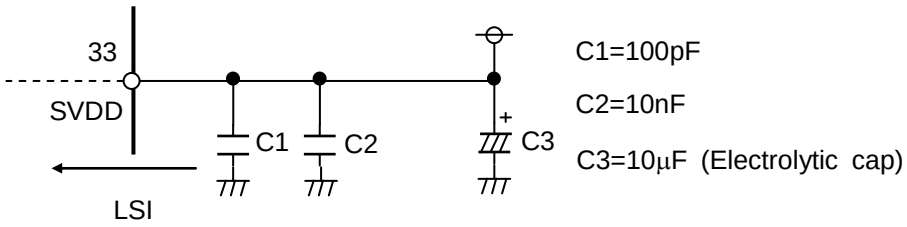
12. Recommended External Circuits

1) Power supply stabilizing capacitors
Connecting capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.

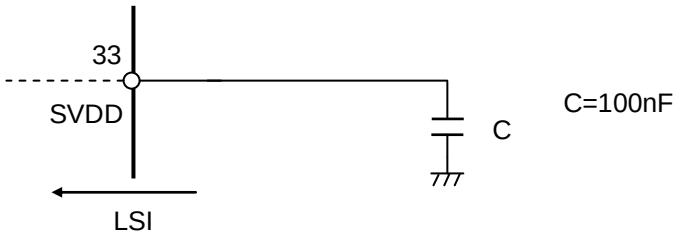


C1=100pF
C2=10nF
C3=10μF (Electrolytic cap)

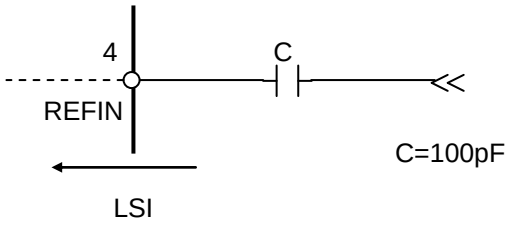
2) SVDD
External Power Supply: IFSEL pin is connected to the ground plane



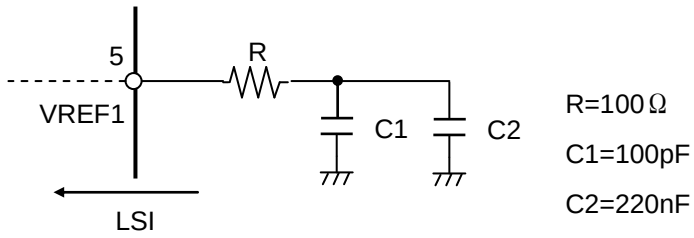
Internal Regulator: IFSEL pin is connected to PVDD



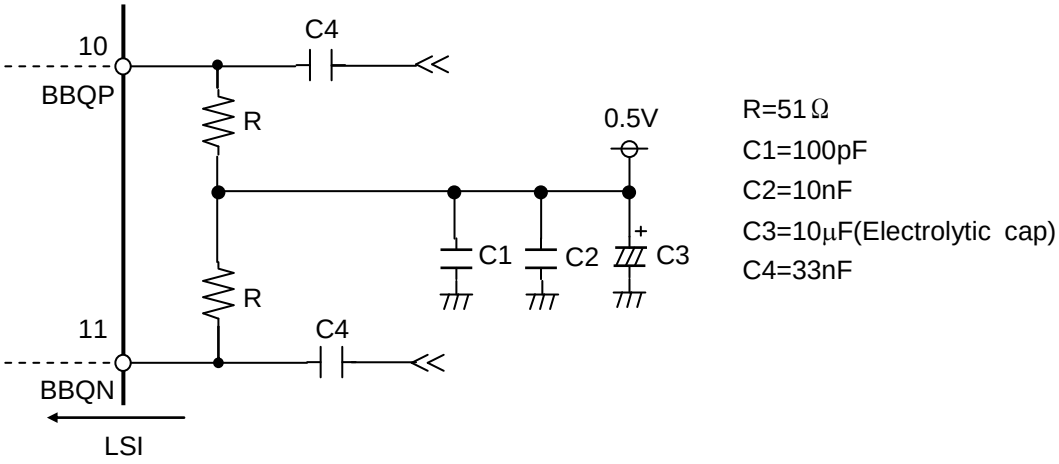
3) REFIN



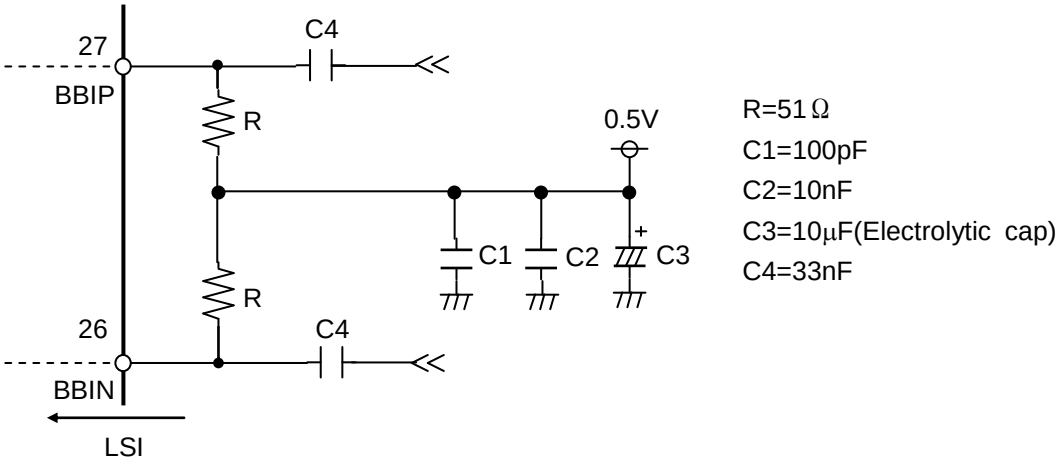
4) VREF1



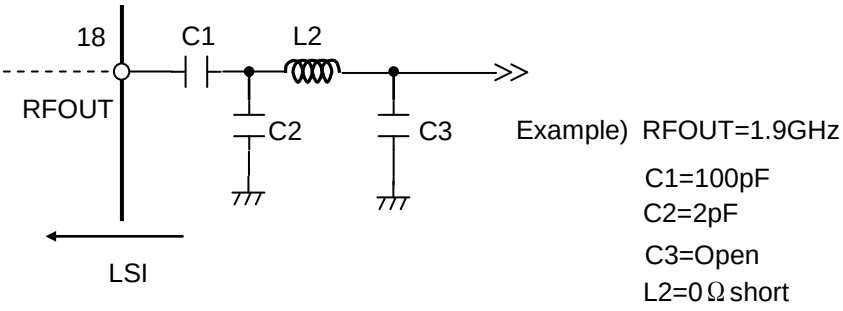
5) BBQP, BBQN



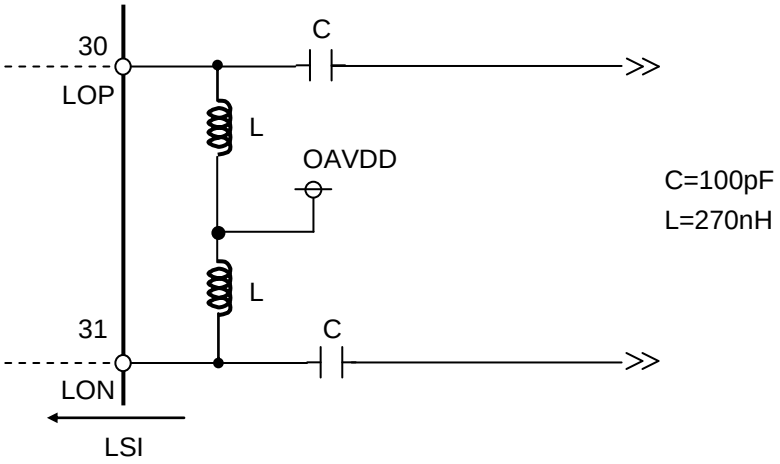
6) BBIP, BBIN



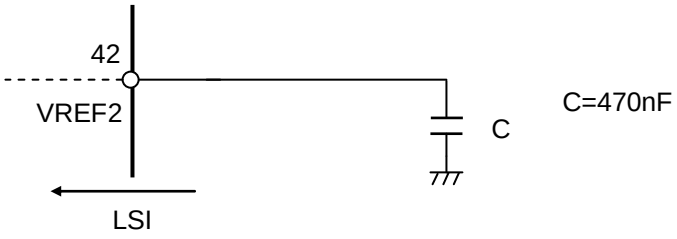
7) RFOUT



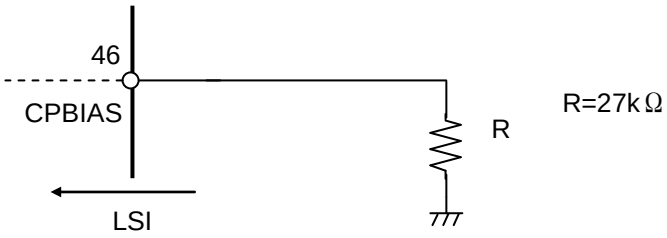
8) LOP, LON



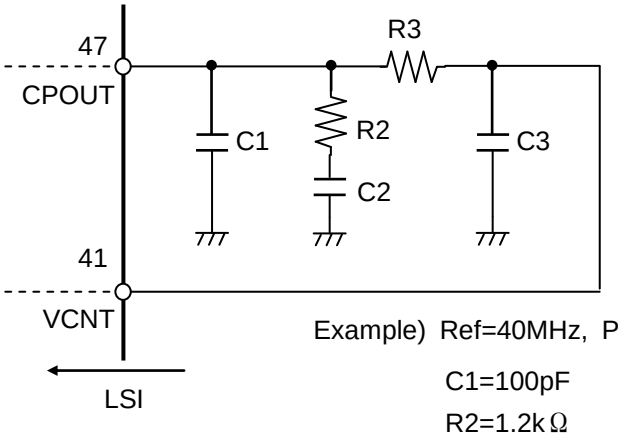
9) VREF2



8) CPBIAS

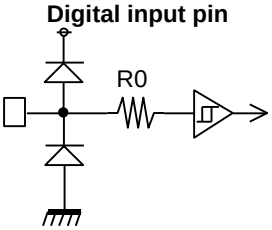
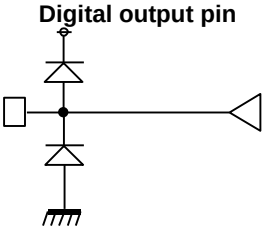
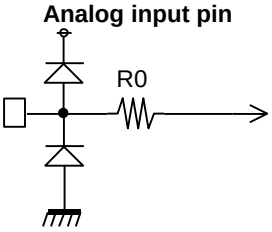


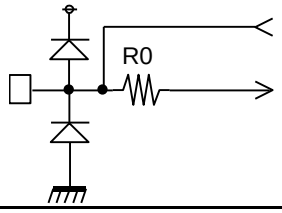
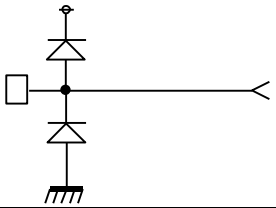
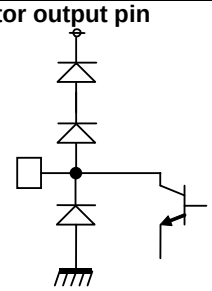
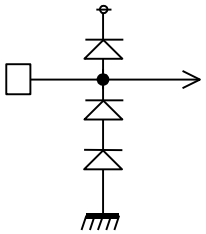
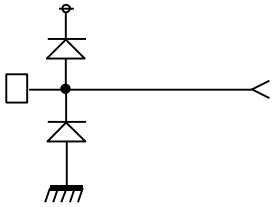
9) CPOUT, VCNT



Example) Ref=40MHz, PFD=40MHz, Rdiv=1, CP1=900µA
C1=100pF
R2=1.2kΩ
C2=8.2nF
R3=1kΩ
C3=100pF

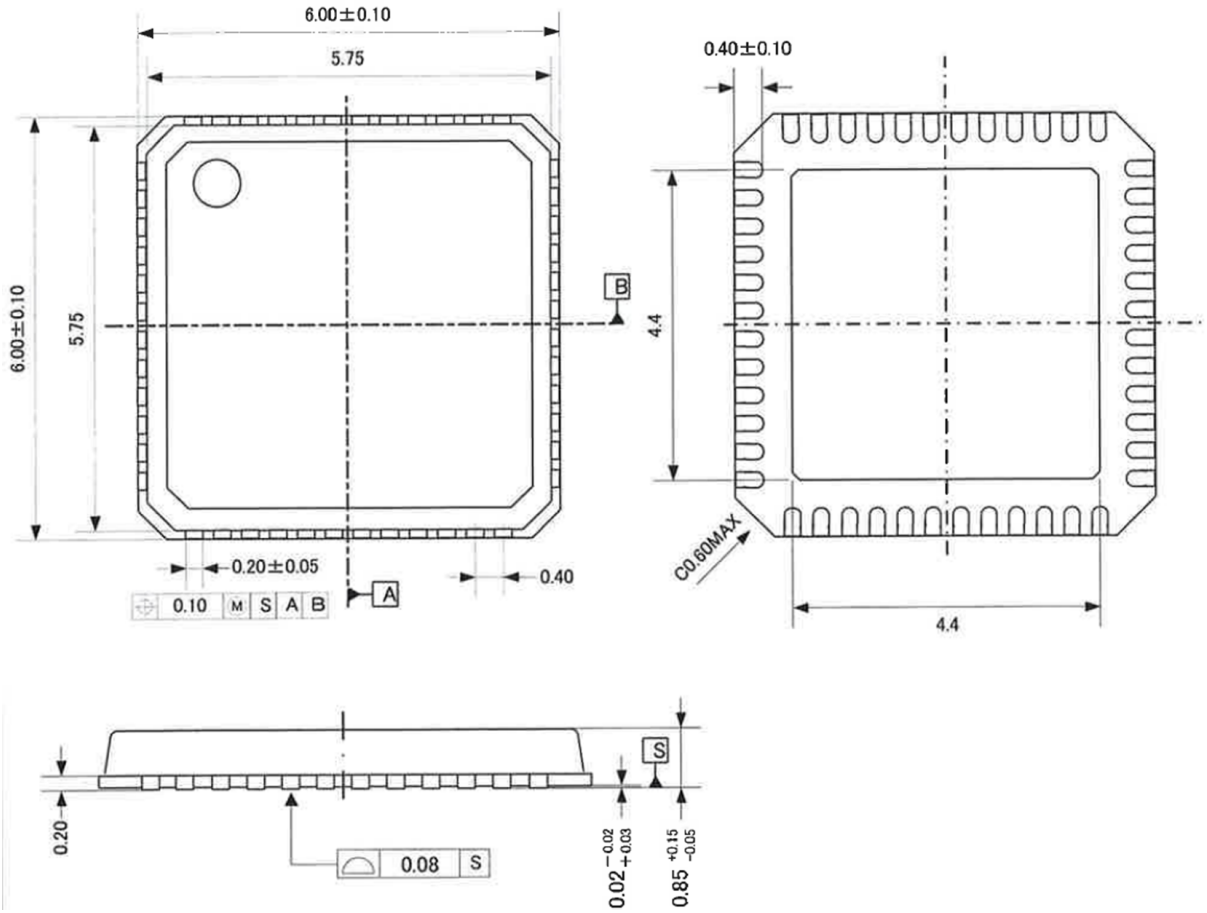
13. LSI Interface Schematic

No.	Pin name	I/O	R0 (Ω)	Function
40	PDN	I	300	**Digital input pin** 
36	TXON	I	300	
35	CLK	I	300	
34	DATA	I	300	
38	LE	I	300	
7	IFSEL	I	300	
37	LD	O		**Digital output pin** 
39	DATAO	O		
41	VCNT	I	100	**Analog input pin** 
4	REFIN	I	300	

No.	Pin name	I/O	R0 (Ω)	Function
46	CPBIAS	IO	300	**Analog I/O pin** 
42	VREF2	IO	300	
33	SVDD	IO	300	
5	VREF1	IO	300	
47	CPOUT	O		**Analog output pin** 
30	LOP	IO		**RF open collector output pin** 
31	LON	IO		
10	BBQP	AI		**Analog input pin** 
11	BBQN	AI		
26	BBIN	AI		
27	BBIP	AI		
18	RFOUT	AO		**RF analog output pin** 

14. Package

14.1. Outline Dimensions



Exposed PAD on Back side of the package should be connected to GND

14.2. Marking

a. Style : QFN
b. Number of pins : 48
c. A1 pin marking : ●
d. Product number : 1599V
e. Date code : YMML (4 digits)

Y : Lower one digit of calendar year (2015->5, 2016->6…)
WW : Week
L : LOT identification, given to each product lot (A, B, C…)
-> LOT ID is given in alphabetical order

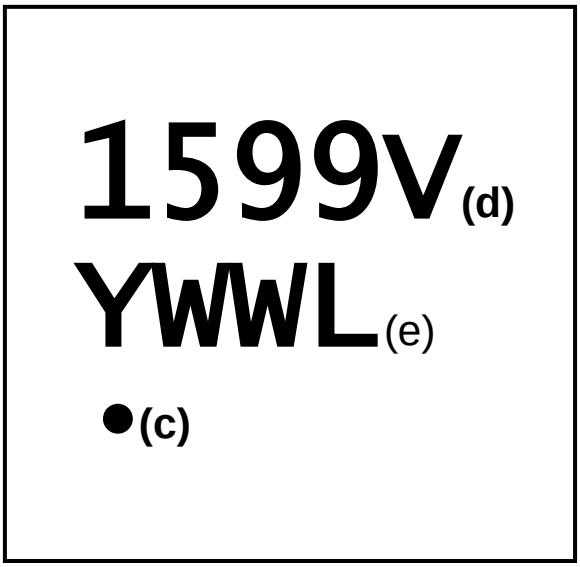
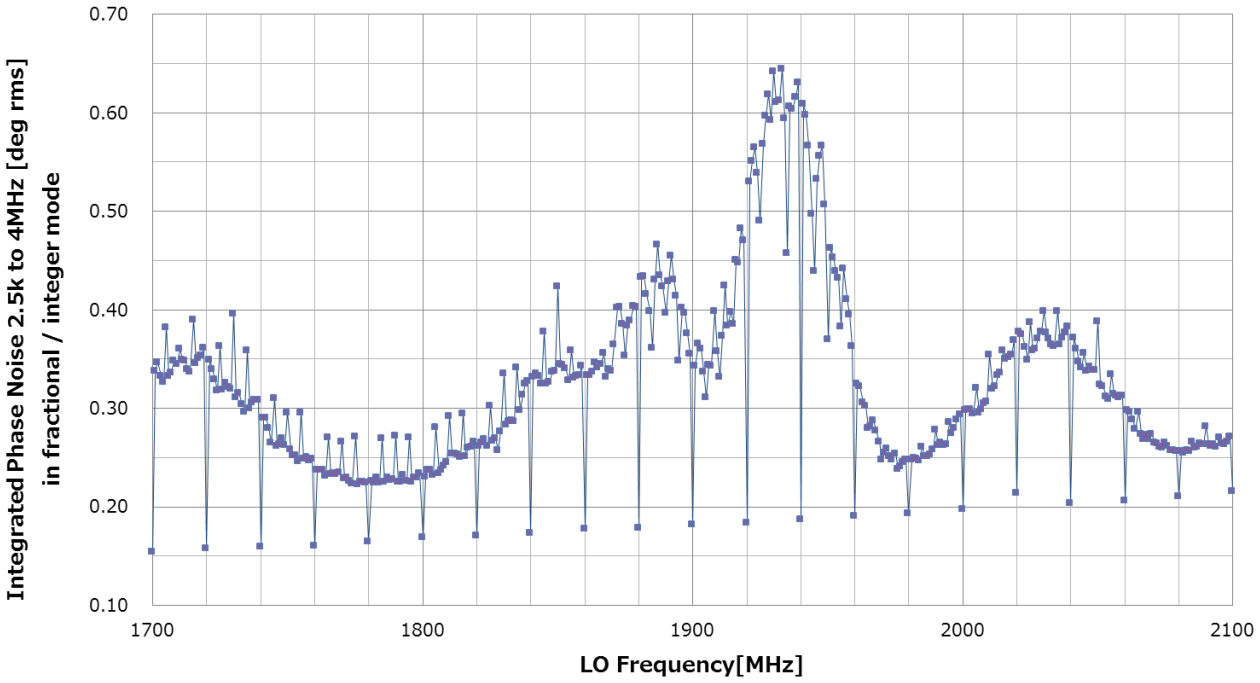


Fig.14 Marking

15. Appendix

Integrated Phase Noise in fractional / integer mode



This graph is example data of one sample.

<Synthesizer setting example>
Measured at 25ºC, VDD2 = VDD3 = 5V
Reference input frequency = 40MHz, 0dBm, R divider = 1, PFD frequency = 40MHz, int = 85 to 105, frac = 0 to 19, mod = 20
Loop Filter: C1 = 100pF, C2 = 8.2nF, C3 = 100pF, R2 = 1.2kΩ, R3 = 1kΩ
CP1 = 600µA in fractional mode and CP1 = 900µA in integer mode.

Fig. 15 Integrated Phase Noise in fractional / integer mode vs. LO frequency

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
2015/5/13	00			

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