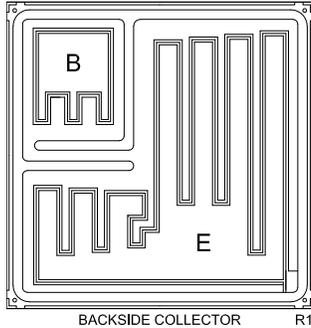


# CP647-PMD19K100

## PNP - Darlington Transistor Die

### 30 Amp, 100 Volt

The CP647-PMD19K100 die is a silicon PNP Darlington power transistor designed for high current applications.



#### MECHANICAL SPECIFICATIONS:

Die Size	211 x 211 MILS
Die Thickness	12.5 MILS
Base Bonding Pad Size	49 x 41 MILS
Emitter Bonding Pad Size	60 x 50 MILS
Top Side Metalization	Al – 50,000Å
Back Side Metalization	Ti/Ni/Ag – 1,000Å/6,000Å/10,000Å
Scribe Alley Width	4 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	246

#### MAXIMUM RATINGS: ( $T_A=25^\circ\text{C}$ )

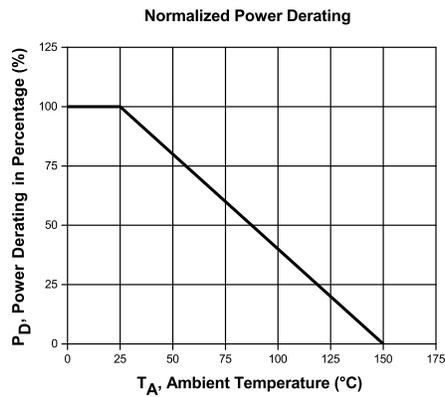
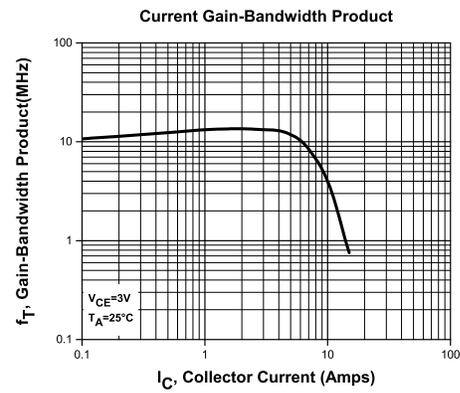
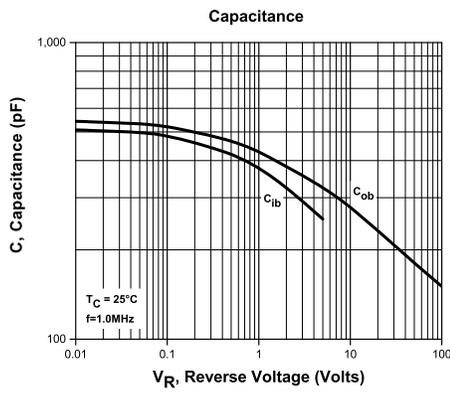
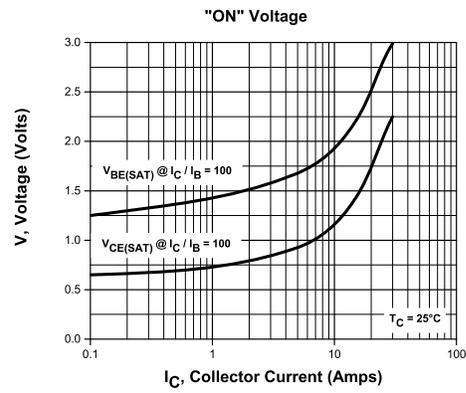
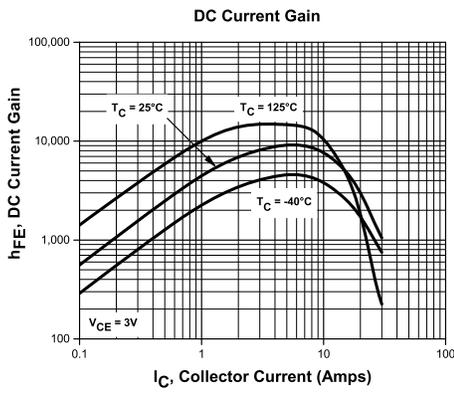
	SYMBOL		UNITS
Collector-Base Voltage	$V_{CBO}$	100	V
Collector-Emitter Voltage	$V_{CER}$	100	V
Collector-Emitter Voltage	$V_{CEO}$	100	V
Emitter-Base Voltage	$V_{EBO}$	5.0	V
Continuous Collector Current	$I_C$	30	A
Peak Collector Current	$I_{CM}$	60	A
Continuous Base Current	$I_B$	750	mA
Operating and Storage Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

#### ELECTRICAL CHARACTERISTICS: ( $T_C=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$I_{CER}$	$V_{CE}=67\text{V}, R_{BE}=2.2\text{k}\Omega$		10	mA
$I_{EBO}$	$V_{EB}=5.0\text{V}$		3.0	mA
$BV_{CER}$	$I_C=100\text{mA}, R_{BE}=2.2\text{k}\Omega$	100		V
$BV_{CEO}$	$I_C=100\text{mA}$	100		V
$V_{CE(SAT)}$	$I_C=15\text{A}, I_B=60\text{mA}$		2.0	V
$V_{BE(SAT)}$	$I_C=15\text{A}, I_B=60\text{mA}$		2.8	V
$V_{BE(ON)}$	$V_{CE}=3.0\text{V}, I_C=15\text{A}$		2.8	V
$h_{FE}$	$V_{CE}=3.0\text{V}, I_C=15\text{A}$	800	20K	
$h_{fe}$	$V_{CE}=3.0\text{V}, I_C=9.0\text{A}, f=1.0\text{kHz}$	300		
$f_T$	$V_{CE}=3.0\text{V}, I_C=9.0\text{A}, f=1.0\text{MHz}$	4.0		MHz
$C_{ob}$	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		600	pF

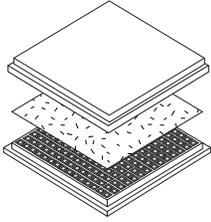
# CP647-PMD19K100

## Typical Electrical Characteristics



## BARE DIE PACKING OPTIONS

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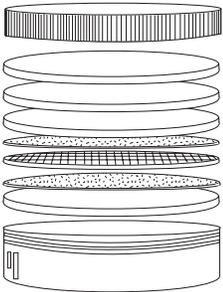


### BARE DIE IN TRAY (WAFFLE) PACK

**CT:** Singulated die in tray (waffle) pack.  
(example: CP211-PART NUMBER-CT)

**CM:** Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).  
(example: CP211-PART NUMBER-CM)

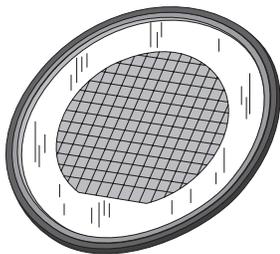
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### UNSAWN WAFER

**WN:** Full wafer, unsawn, 100% tested with reject die inked.  
(example: CP211-PART NUMBER-WN)

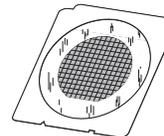
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### SAWN WAFER ON PLASTIC RING

**WR:** Full wafer, sawn and mounted on plastic ring,  
100% tested with reject die inked.  
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:  
[www.centrasemi.com/bdspecs](http://www.centrasemi.com/bdspecs)

R2 (3-April 2017)

## OUTSTANDING SUPPORT AND SUPERIOR SERVICES



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### PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

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### DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

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### CONTACT US

#### Corporate Headquarters & Customer Support Team

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