ALLIANCE MEMORY

256K X 36, 512K X 18
3.3V Synchronous SRAMs
3.3V I/O, Burst Counter
Flow-Through Outputs, Single Cycle Deselect

AS8C803625
AS8C801825

Features

- **256K x 36, 512K x 18 memory configuration**
- **Supports fast access times:**
  - *7.5ns up to 117MHz clock frequency*
- **$\overline{\text{LBO}}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{\text{GW}}$), byte write enable ($\overline{\text{BWE}}$), and byte writes ($\overline{\text{BW}}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **3.3V I/O supply (V_{DDQ})**
- **Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP)**

Description

The 803625/801825 are high-speed SRAMs organized as 256K x 36/512K x 18. The 803625/801825 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the 803625/801825 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{\text{ADV}}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The orders of these three addresses are defined by the internal burst counter and the $\overline{\text{LBO}}$ input pin.

The 803625/801825 SRAMs utilize Alliance's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP).

Pin Description Summary

$A_0 – A_{18}$	Address Inputs	Input	Synchronous
$\overline{\text{CE}}$	Chip Enable	Input	Synchronous
CS_0, $\overline{\text{CS}}_1$	Chip Selects	Input	Synchronous
$\overline{\text{OE}}$	Output Enable	Input	Asynchronous
$\overline{\text{GW}}$	Global Write Enable	Input	Synchronous
$\overline{\text{BWE}}$	Byte Write Enable	Input	Synchronous
$\overline{\text{BW}}_1$, $\overline{\text{BW}}_2$, $\overline{\text{BW}}_3$, $\overline{\text{BW}}_4$ (1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{\text{ADV}}$	Burst Address Advance	Input	Synchronous
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{\text{ADSP}}$	Address Status (Processor)	Input	Synchronous
$\overline{\text{LBO}}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
$I/O_0 – I/O_{31}$, $I/O_{P1} – I/O_{P4}$	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

5309 tbl 01

NOTE:
1. $\overline{\text{BW}}_3$ and $\overline{\text{BW}}_4$ are not applicable for 803625/801825.

NOVEMBER 2010

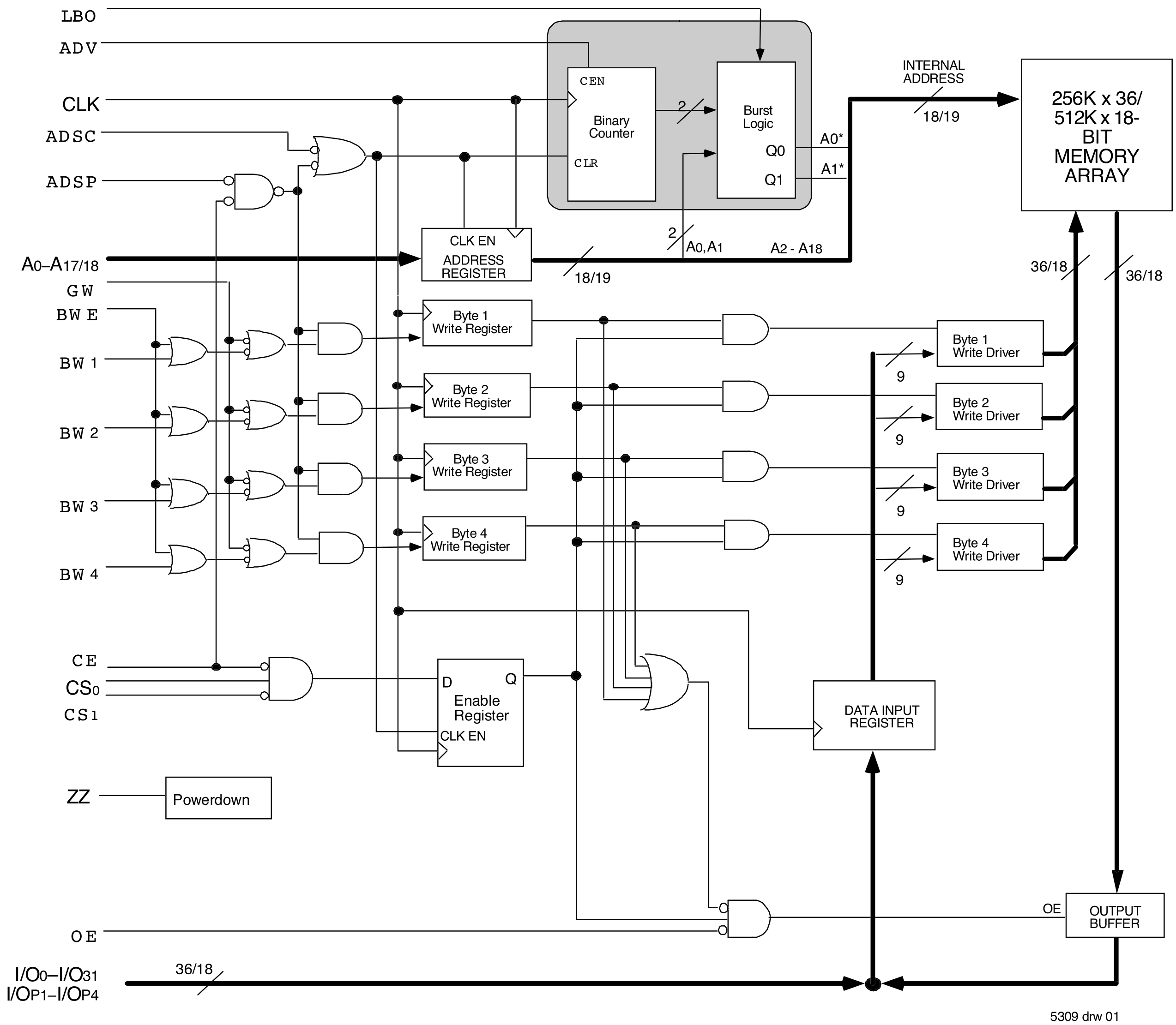
Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combi-nation of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW_x}$ inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O_{0-7}, I/O_{P1}, $\overline{BW_2}$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable AS8C803625/801825. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the inter-leaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	1	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C803625/801825 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

5309 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Absolute Maximum Ratings[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A[7]	Operating Temperature	-0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5309 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature Supply Voltage

Grade	Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5309 tbl 04

NOTE:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5309 tbl 05

NOTE:
1. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100-Pin TQFP Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07

119 BGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07a

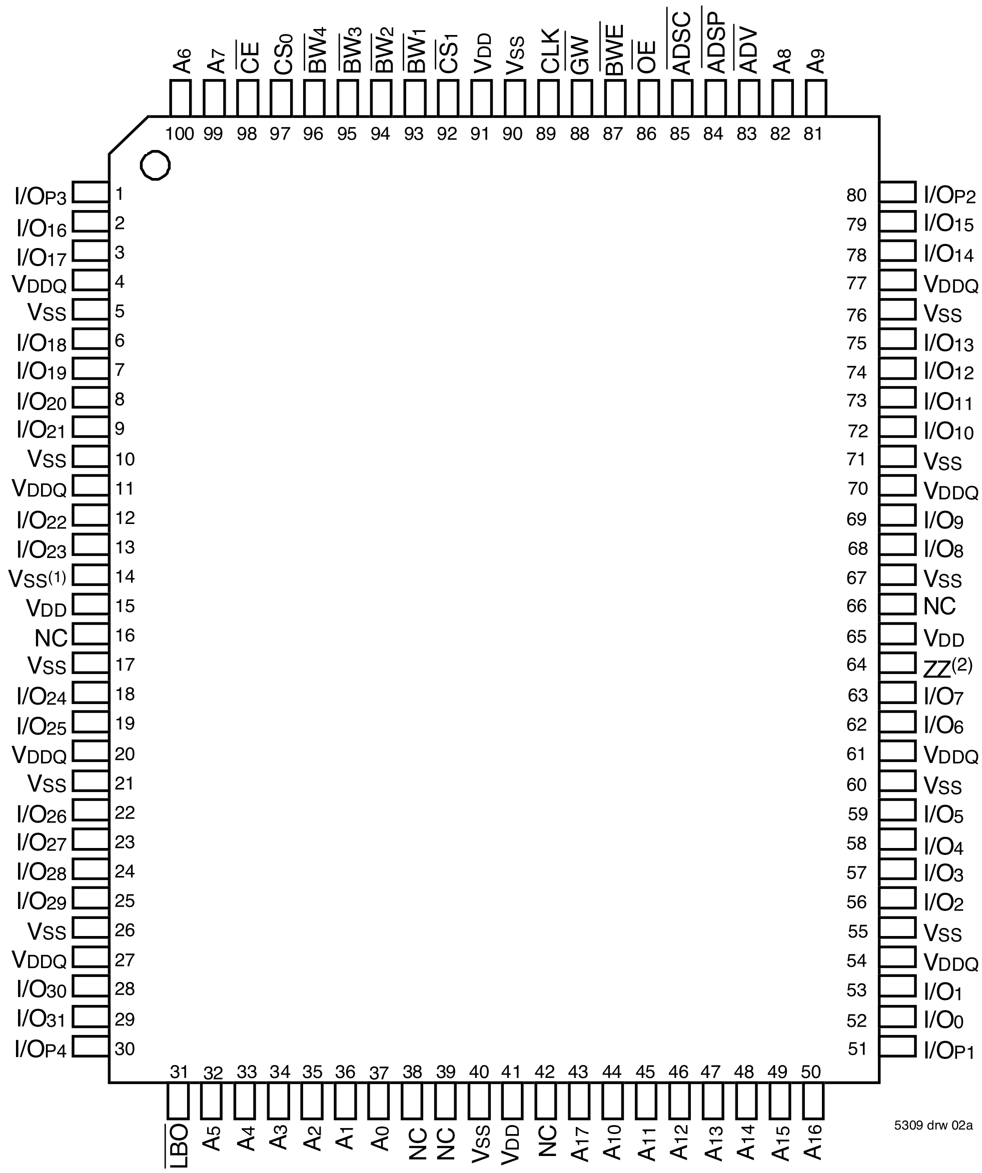
165 fBGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration – 256K x 36, 100-Pin TQFP

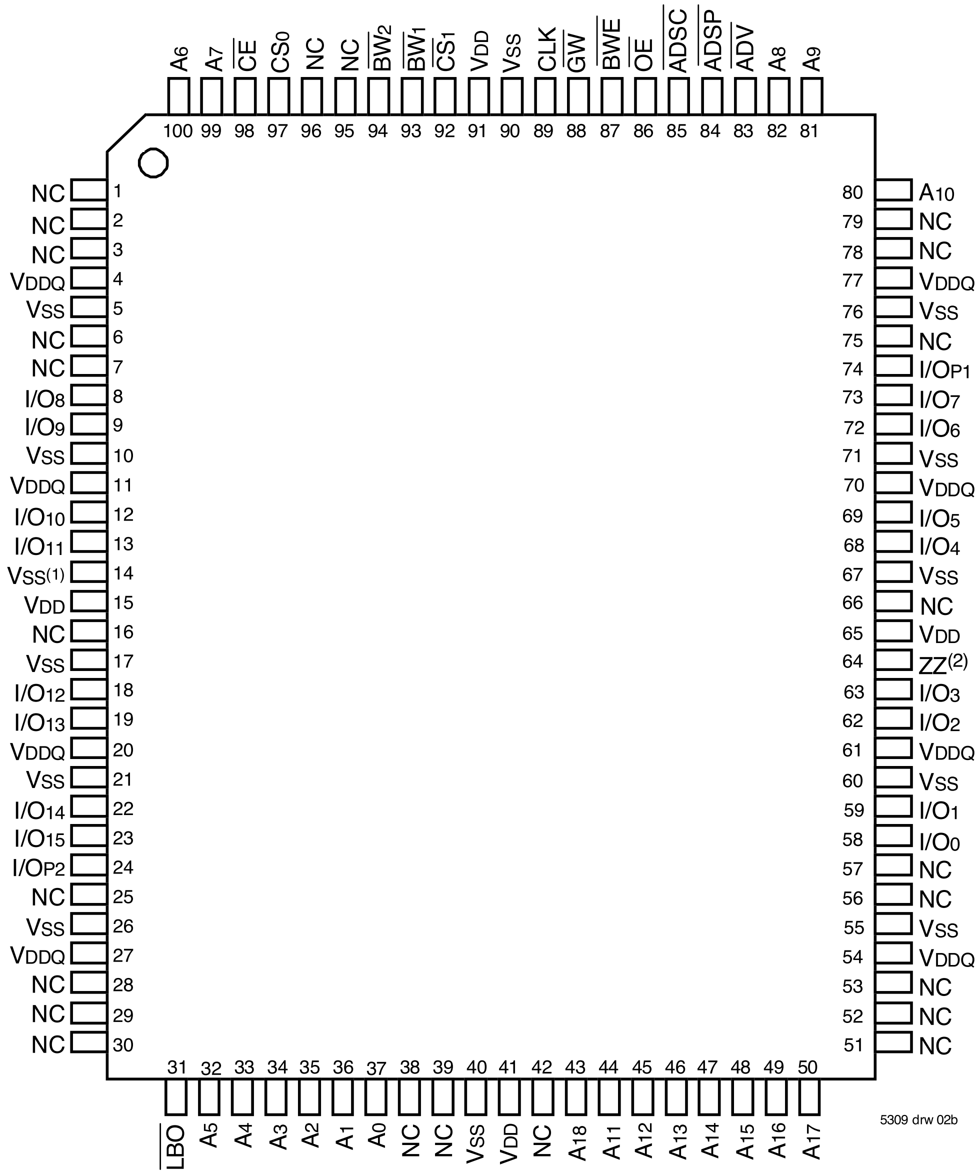


Top View

NOTES:

1. Pin 14 does not have to be directly connected to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 512K x 18, 100-Pin TQFP



Top View

NOTES:

1. Pin 14 does not have to be directly connected to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 256K x 36, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	$\overline{\text{ADSP}}$	A8	A16	VDDQ
B	NC	CS0(4)	A3	$\overline{\text{ADSC}}$	A9	A17	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	$\overline{\text{CE}}$	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	$\overline{\text{OE}}$	VSS	I/O12	VDDQ
G	I/O20	I/O21	$\overline{\text{BW3}}$	$\overline{\text{ADV}}$	$\overline{\text{BW2}}$	I/O11	I/O10
H	I/O22	I/O23	VSS	$\overline{\text{GW}}$	VSS	I/O9	I/O8
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	$\overline{\text{BW4}}$	NC	$\overline{\text{BW1}}$	I/O4	I/O5
M	VDDQ	I/O28	VSS	$\overline{\text{BWE}}$	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	$\overline{\text{LBO}}$	VDD	VSS(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ(2)
U	VDDQ	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	VDDQ

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Top View

Pin Configuration – 512K x 18, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	$\overline{\text{ADSP}}$	A8	A16	VDDQ
B	NC	CS0(4)	A3	$\overline{\text{ADSC}}$	A9	A18	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	$\overline{\text{CE}}$	VSS	NC	I/O7
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	I/O6	VDDQ
G	NC	I/O10	$\overline{\text{BW2}}$	$\overline{\text{ADV}}$	VSS	NC	I/O5
H	I/O11	NC	VSS	$\overline{\text{GW}}$	VSS	I/O4	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	$\overline{\text{BW1}}$	I/O2	NC
M	VDDQ	I/O14	VSS	$\overline{\text{BWE}}$	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	$\overline{\text{LBO}}$	VDD	VSS(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ(2)
U	VDDQ	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	VDDQ

5309 drw 02d

Top View

NOTES:

1. R5 does not have to be directly connected to VSS as long as the input voltage is ≤ VIL.
2. T7 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to VSS.
4. On future 18M devices CS_0 will be removed, B2 will be used for address expansion.

Pin Configuration – 256K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC[3]	A_7	$\overline{CE}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A_8	NC
B	NC	A_6	CS_0	$\overline{BW_4}$	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A_9	NC[3]
C	I/O$_{P3}$	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	I/O$_{P2}$
D	I/O$_{17}$	I/O$_{16}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_{15}$	I/O$_{14}$
E	I/O$_{19}$	I/O$_{18}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_{13}$	I/O$_{12}$
F	I/O$_{21}$	I/O$_{20}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_{11}$	I/O$_{10}$
G	I/O$_{23}$	I/O$_{22}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_9$	I/O$_8$
H	V_{SS}[1]	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ[2]
J	I/O$_{25}$	I/O$_{24}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_7$	I/O$_6$
K	I/O$_{27}$	I/O$_{26}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_5$	I/O$_4$
L	I/O$_{29}$	I/O$_{28}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_3$	I/O$_2$
M	I/O$_{31}$	I/O$_{30}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_1$	I/O$_0$
N	I/O$_{P4}$	NC	V_{DDQ}	V_{SS}	NC	NC[3]	NC	V_{SS}	V_{DDQ}	NC	I/O$_{P1}$
P	NC	NC[3]	A_5	A_2	DNU[4]	A_1	DNU[4]	A_{10}	A_{13}	A_{14}	A_{17}
R	$\overline{LBO}$	NC[3]	A_4	A_3	DNU[4]	A_0	DNU[4]	A_{11}	A_{12}	A_{15}	A_{16}

5309tbl 17a

Pin Configuration – 512K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC[3]	A_7	$\overline{CE}$	$\overline{BW_2}$	NC	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A_8	A_{10}
B	NC	A_6	CS_0	NC	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A_9	NC[3]
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	I/O$_{P1}$
D	NC	I/O$_8$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O$_7$
E	NC	I/O$_9$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O$_6$
F	NC	I/O$_{10}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O$_5$
G	NC	I/O$_{11}$	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	I/O$_4$
H	V_{SS}[1]	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ[2]
J	I/O$_{12}$	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_3$	NC
K	I/O$_{13}$	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_2$	NC
L	I/O$_{14}$	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_1$	NC
M	I/O$_{15}$	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	I/O$_0$	NC
N	I/O$_{P2}$	NC	V_{DDQ}	V_{SS}	NC	NC[3]	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC[3]	A_5	A_2	DNU[4]	A_1	DNU[4]	A_{11}	A_{14}	A_{15}	A_{18}
R	$\overline{LBO}$	NC[3]	A_4	A_3	DNU[4]	A_0	DNU[4]	A_{12}	A_{13}	A_{16}	A_{17}

5309 tbl 17b

NOTES:
1. H1 does not have to be directly connected to V_{SS}, as long as the input voltage is $\leq V_{IL}$.
2. H11 can be left unconnected and the device will always remain in active mode.
3. Pin N6, B11, A1, R2 and P2 are reserved for 18M, 36M, 72M, and 144M and 288M respectively.
4. DNU= Do not use; these signals can either be left unconnected or tied to V_{SS}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5309 tbl 08

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ in will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (1)

Symbol	Parameter	Test Conditions	7.5ns		8ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	265	285	210	230	190	210	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	50	70	50	70	50	70	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX} (2,,3)	145	165	140	160	135	155	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	50	70	50	70	50	70	mA

5309 tbl 09

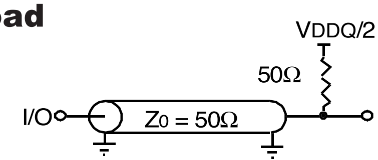
NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 3.3V/2.5V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

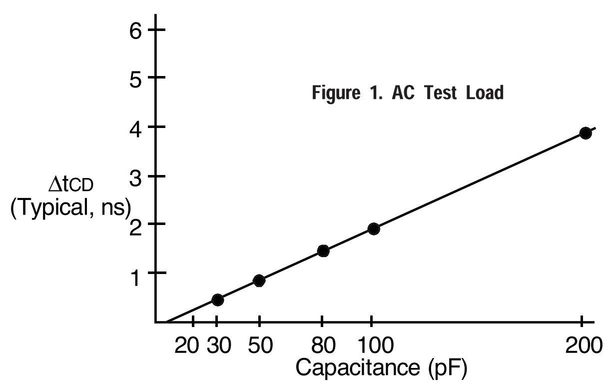
5309 tbl 10

AC Test Load



5309 drw 03

Figure 1. AC Test Load



5309 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table (1,3)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_x}$	$\overline{OE}$(2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	D_{IN}
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	D_{IN}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	D_{IN}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	D_{IN}

5309 tbl 11

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ - low for the table.

Synchronous Write Function Truth Table (1, 2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1[3]	H	L	L	H	H	H
Write Byte 2[3]	H	L	H	L	H	H
Write Byte 3[3]	H	L	H	H	L	H
Write Byte 4[3]	H	L	H	H	H	L

5309 tbl 12

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V67903.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table (1)

Operation[2]	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5309 tbl 13

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	1	0	0	1	0	0

5309 tbl 14

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	0	0	0	1	1	0

5309 tbl 15

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

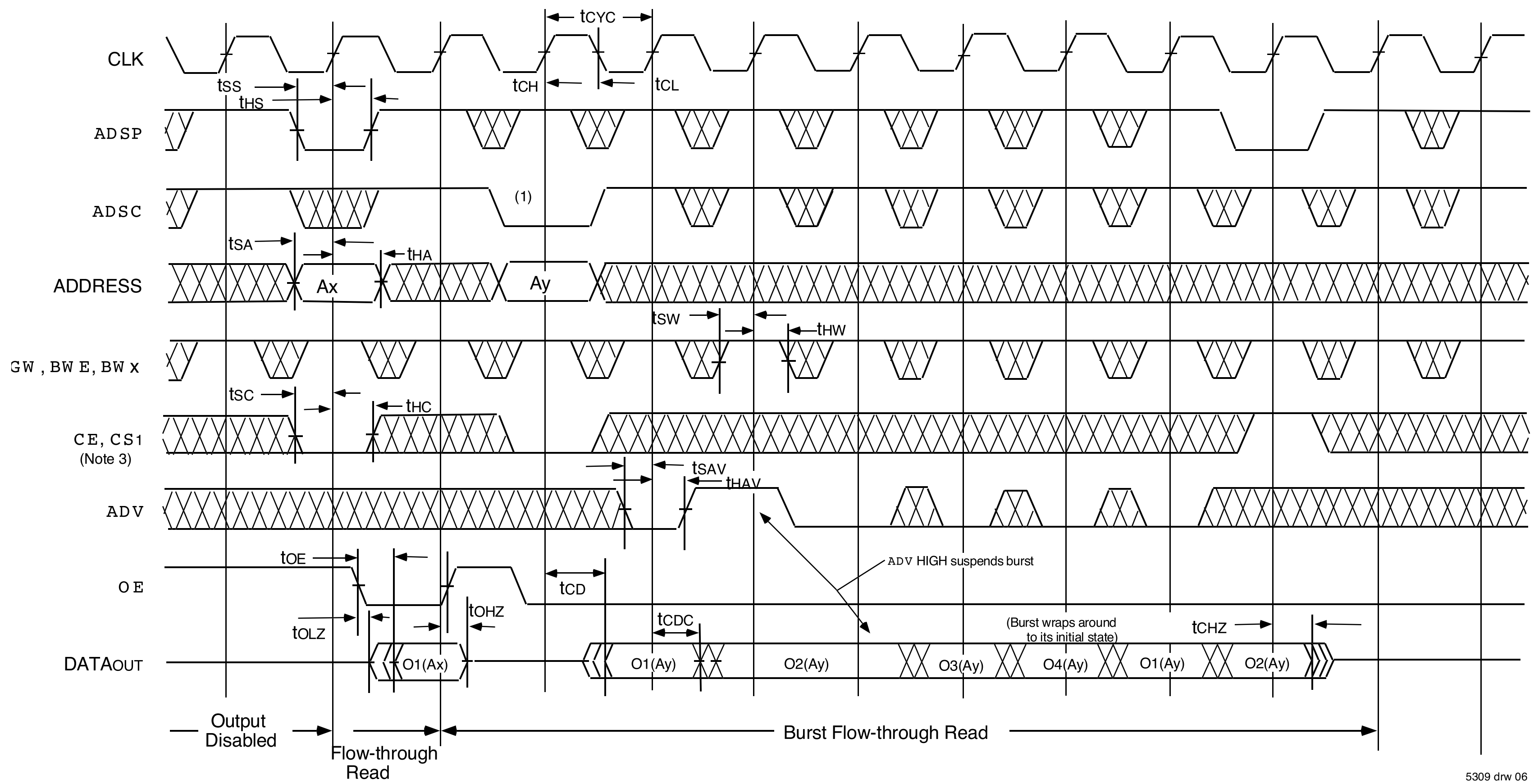
AC Electrical Characteristics (V_{DD} = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	7.5ns		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameter								
t_{CYC}	Clock Cycle Time	8.5	—	10	—	11.5	—	ns
t_{CH}(1)	Clock High Pulse Width	3	—	4	—	4.5	—	ns
t_{CL}(1)	Clock Low Pulse Width	3	—	4	—	4.5	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	2	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	2	3.5	2	3.5	2	3.5	ns
t_{OE}	Output Enable Access Time	—	3.5	—	3.5	—	3.5	ns
t_{OLZ}(2)	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Output High-Z	—	3.5	—	3.5	—	3.5	ns
Set Up Times								
t_{SA}	Address Setup Time	1.5	—	2	—	2	—	ns
t_{SS}	Address Status Setup Time	1.5	—	2	—	2	—	ns
t_{SD}	Data In Setup Time	1.5	—	2	—	2	—	ns
t_{SW}	Write Setup Time	1.5	—	2	—	2	—	ns
t_{SAV}	Address Advance Setup Time	1.5	—	2	—	2	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	2	—	2	—	ns
Hold Times								
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	34	—	40	—	50	—	ns

5309 tbl 16

NOTES:
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

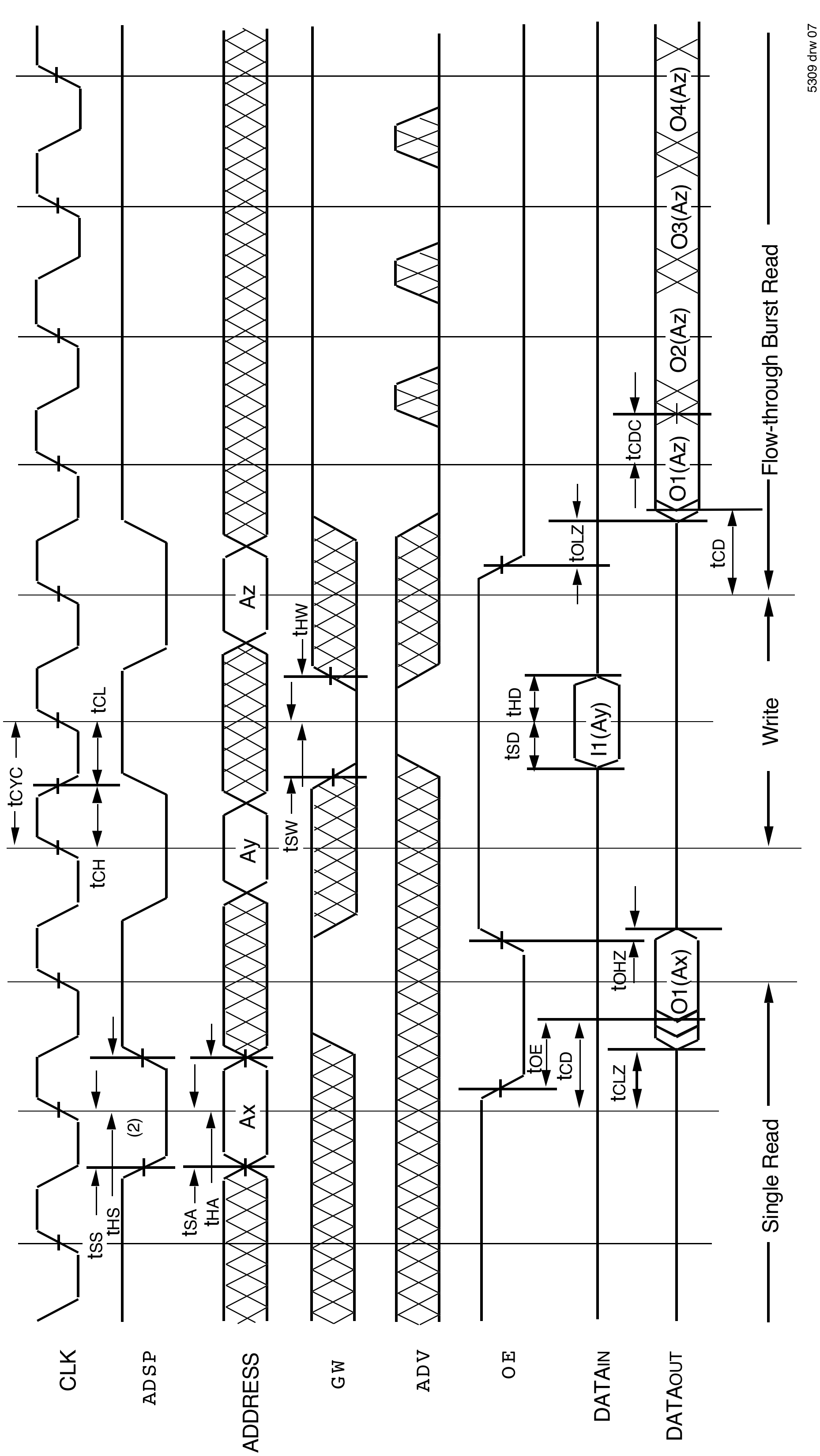
Timing Waveform of Flow-Through Read Cycle (1,2)



NOTES:

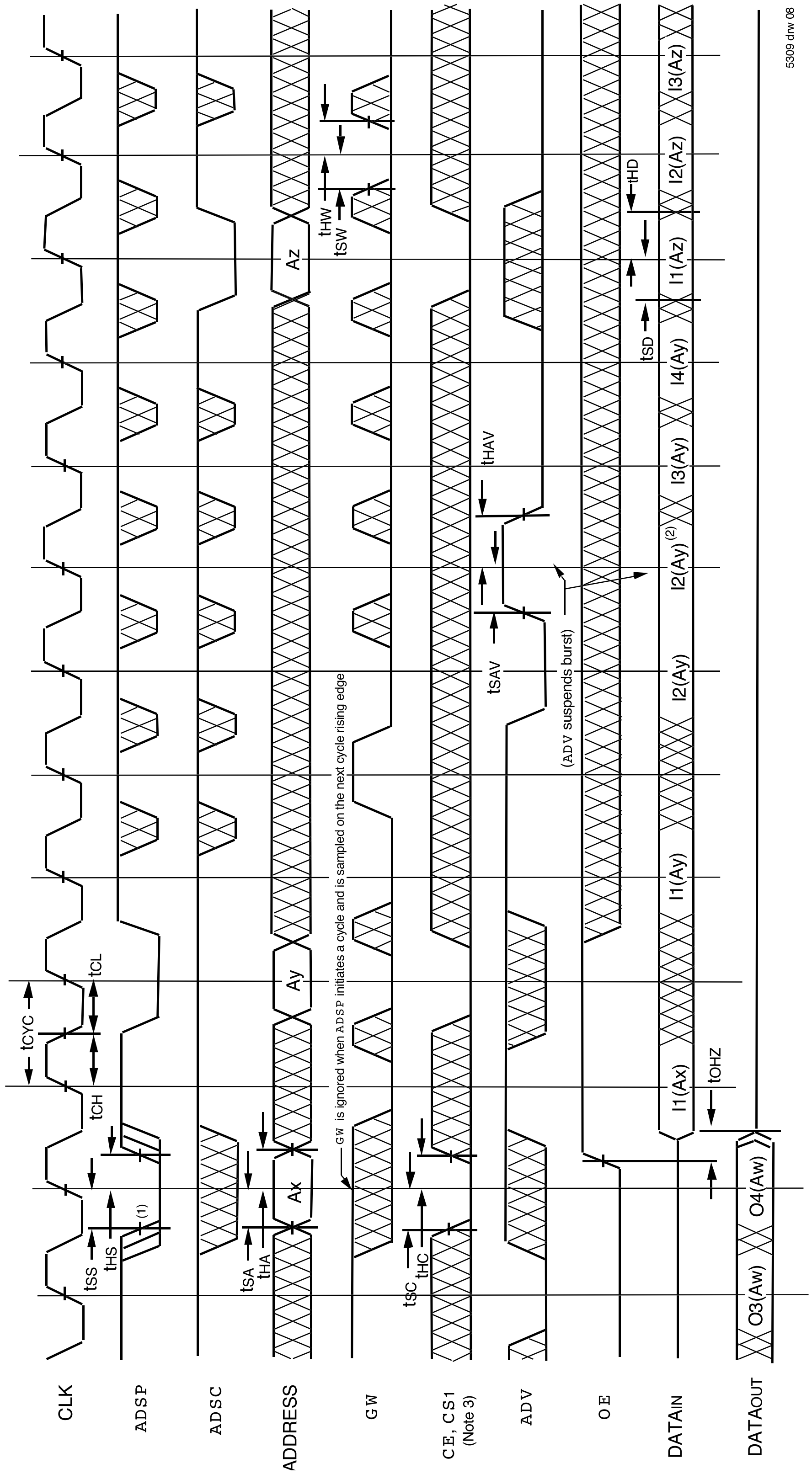
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Combined Flow-Through Read and Write Cycles (1,2,3)



NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS1}$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

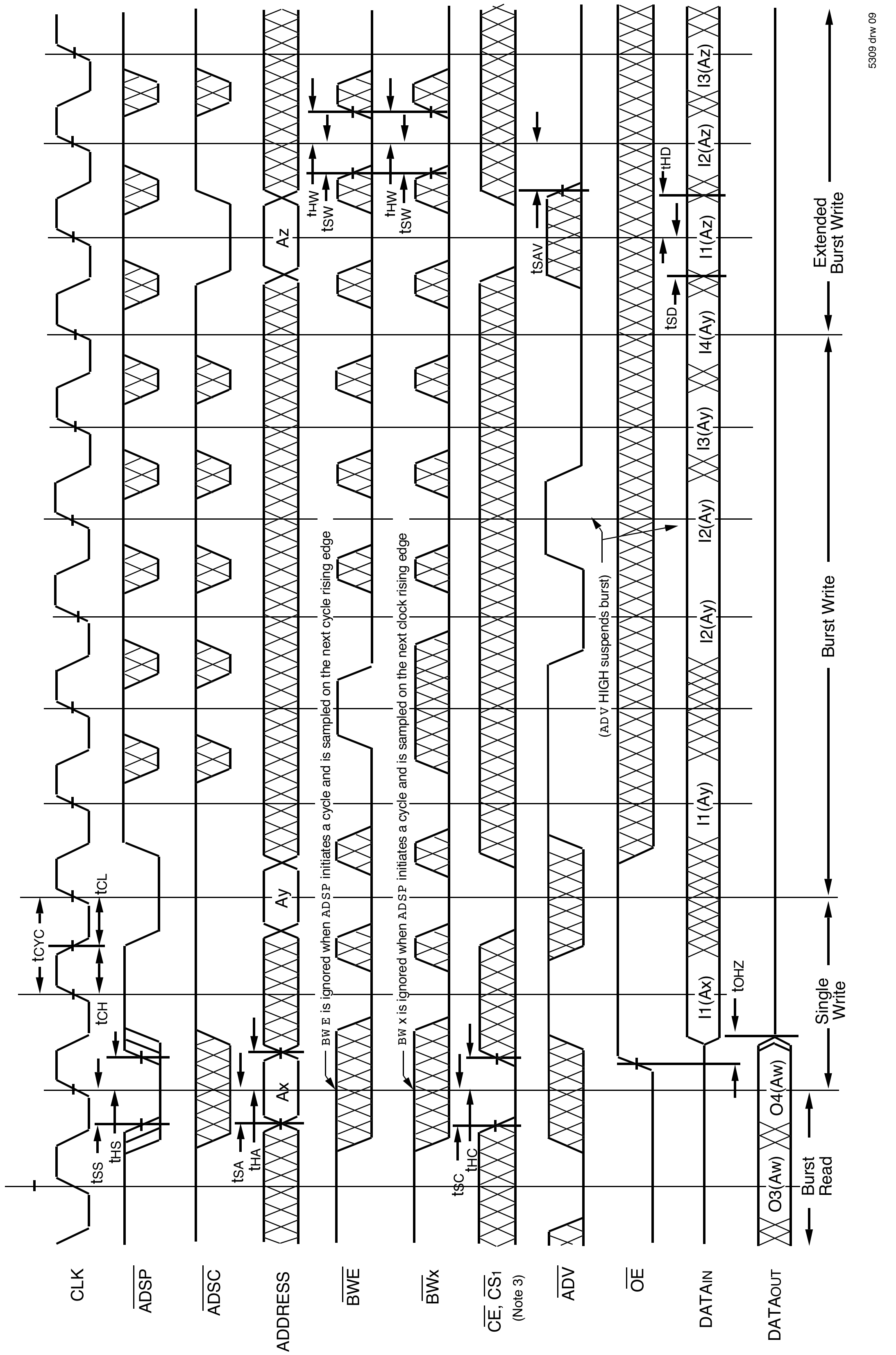
Timing Waveform of Write Cycle No. 1 - $\overline{GW}$ Controlled (1,2,3)



NOTES:

1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

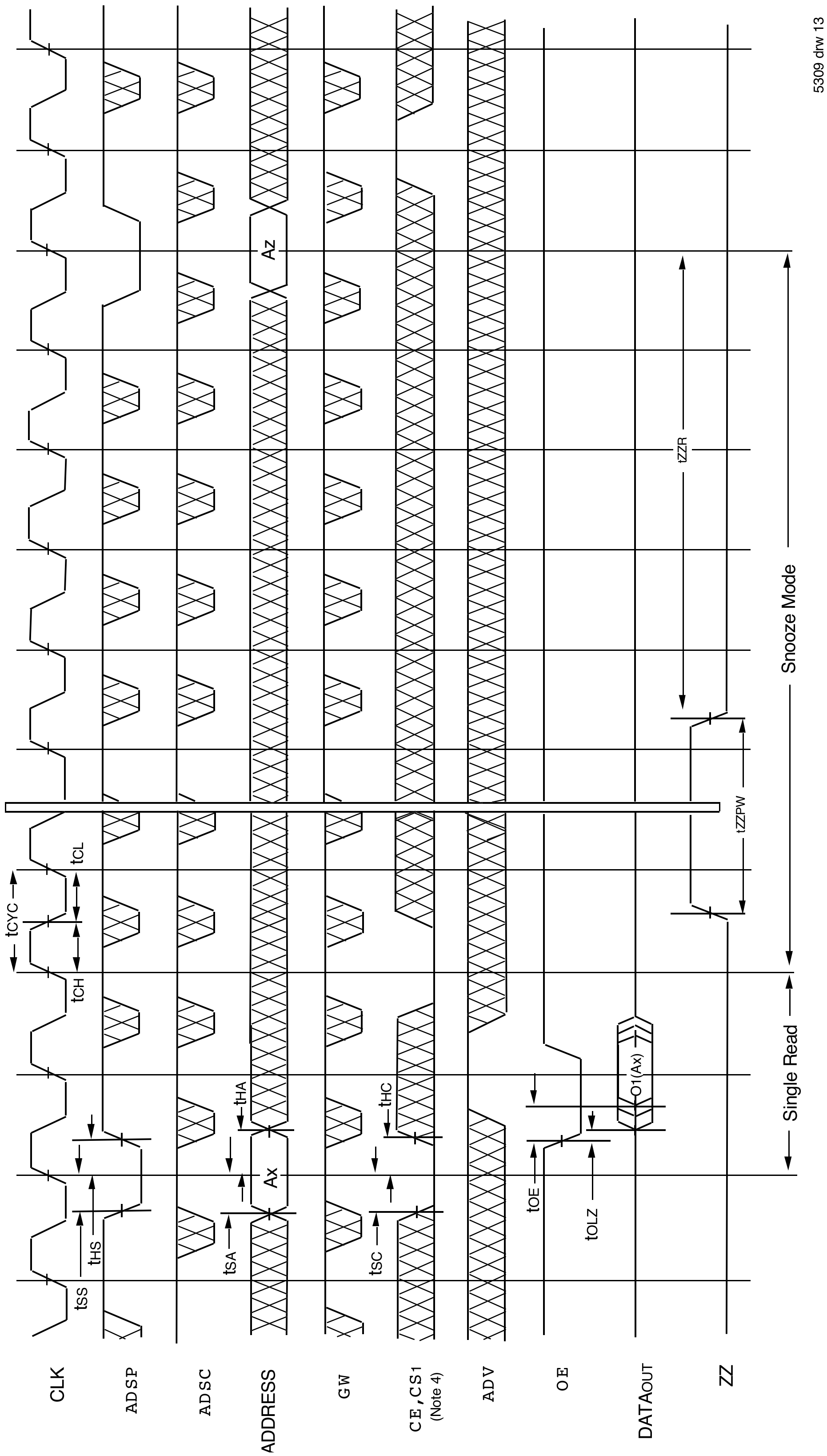
Timing Waveform of Write Cycle No. 2 - Byte Controlled (1,2,3)



NOTES:

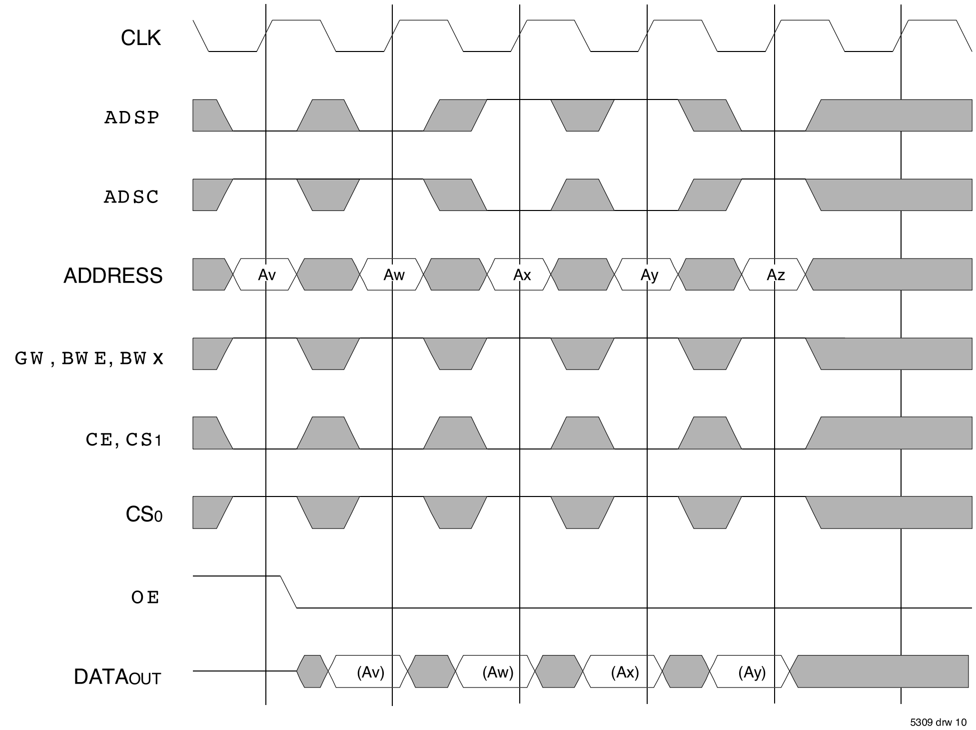
1. ZZ input is LOW, GW is HIGH and LBO is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input. In the case of input I2 (Ay) this data is valid for two cycles because ADV is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes (1,2,3)



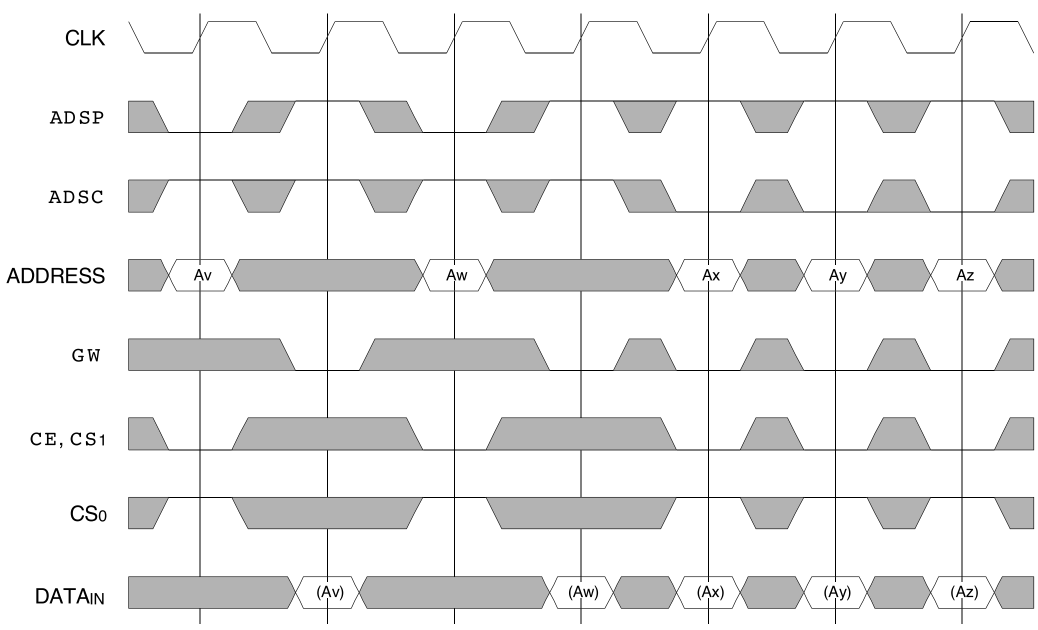
NOTES:
1. Device must power up in deselected Mode.
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform



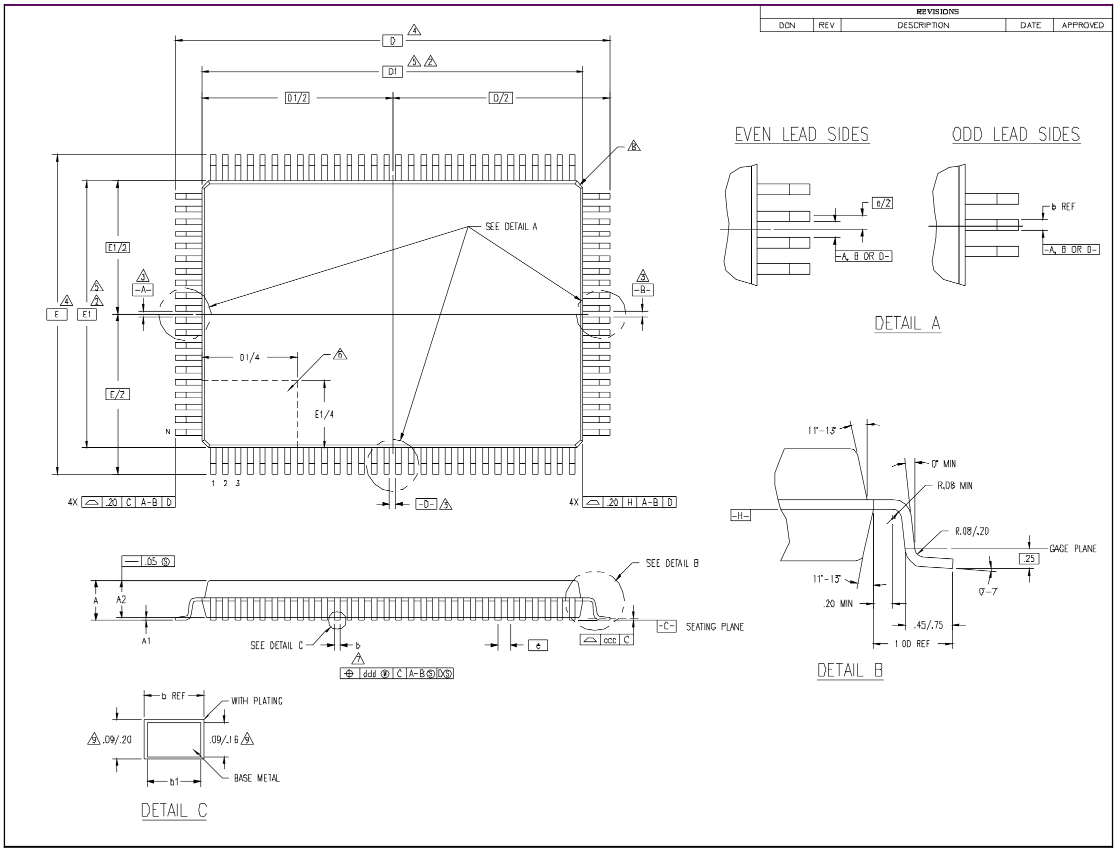
NOTES:
1. ZZ input is LOW, $\overline{ADV}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, $\overline{ADSP}$ and $\overline{ADSC}$ function identically and are therefore interchangable.

Non-Burst Write Cycle Timing Waveform



NOTES:
1. ZZ input is LOW, $\overline{ADV}$ and $\overline{OE}$ are HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only $\overline{GW}$ writes are shown, the functionality of $\overline{BWE}$ and $\overline{BW}$x together is the same as $\overline{GW}$.
4. For write cycles, $\overline{ADSP}$ and $\overline{ADSC}$ have different limitations.

100-Pin Thin Plastic Quad Flatpack (TQFP) Package Diagram Outline



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED

SYMBOL	JEDEC VARIATION DJ MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			4
D1	20.00 BSC			5,2
E	16.00 BSC			4
E1	14.00 BSC			5,2
N	100			
ND	30			
NE	20			
e	.65 BSC			
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	13	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A–B AND -D- TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

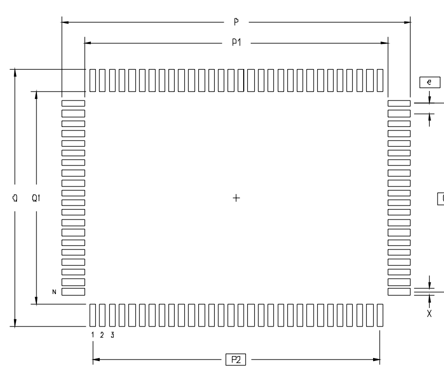
8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–136, VARIATION DJ AND BX

LAND PATTERN DIMENSIONS

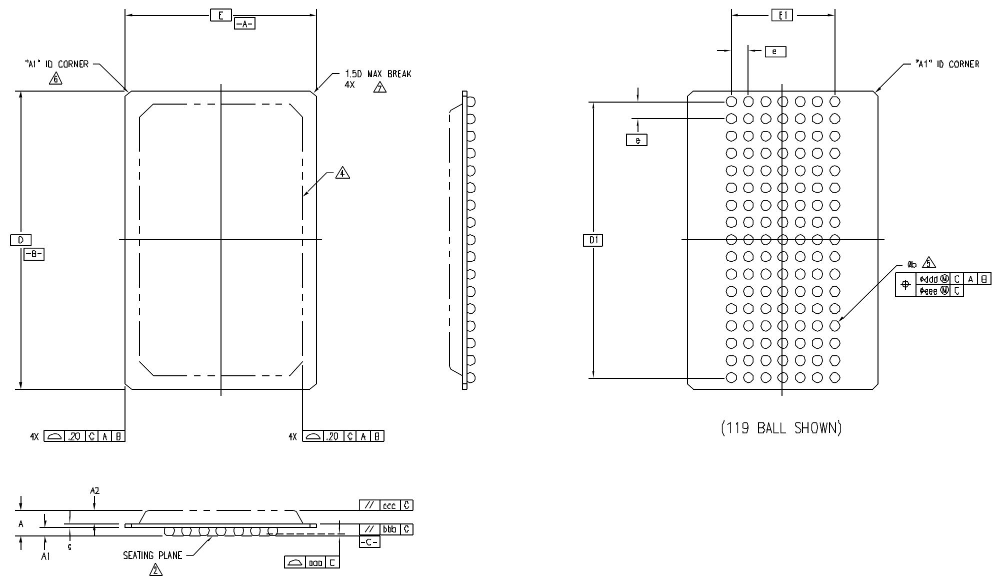


	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

119 Ball Grid Array (BGA) Package Diagram Outline

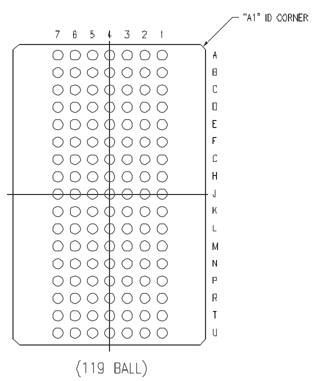
REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	T VU
	02	CHANGE PACKAGE THICKNESS	08/05/00	



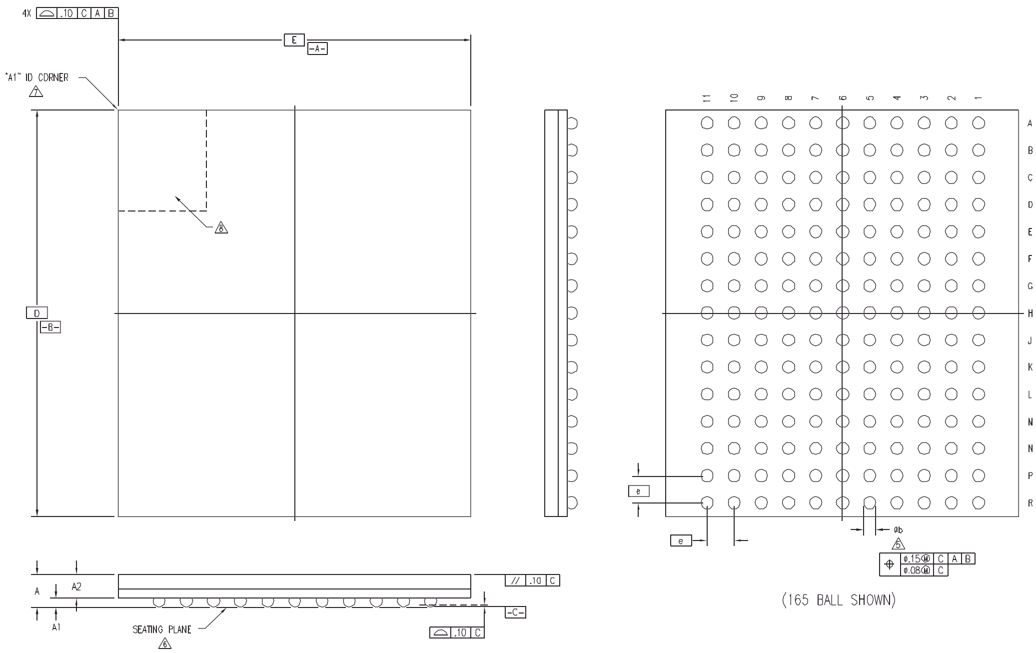
SYMBOL	JEDEC VARIATION AA MIN	NOM	MAX	NOTE
A	–	2.15	2.36	
A1	.50	.60	.70	
A2	–	–	1.20	
D		22.00 BSC		
D1		20.32 BSC		
E		14.00 BSC		
E1		7.62 BSC		
MD		17		3
ME		7		3
N		119		3
e		1.27 BSC		
b	.60	.75	.90	5
c	.51	.56	.61	
aaa	–	–	.15	
bbb	–	–	.25	
ccc	–	–	.35	
ddd	–	–	.30	
eee	–	–	.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
3. "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
"ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
"N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS
4. PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE
7. ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL
8. ALL DIMENSIONS ARE IN MILLIMETERS
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-028, VARIATION AA

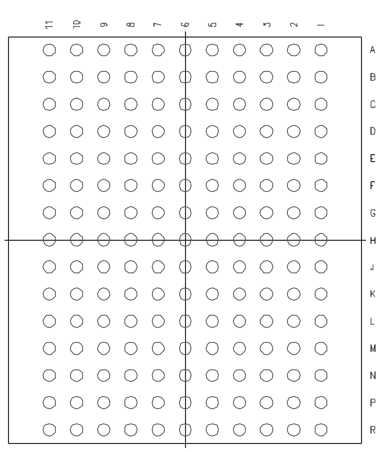
165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	



(165 BALL SHOWN)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	



(165 BALL)

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2 "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH

3 "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE

4 "N" REPRESENTS THE BALLCOUNT NUMBER

5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6 SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

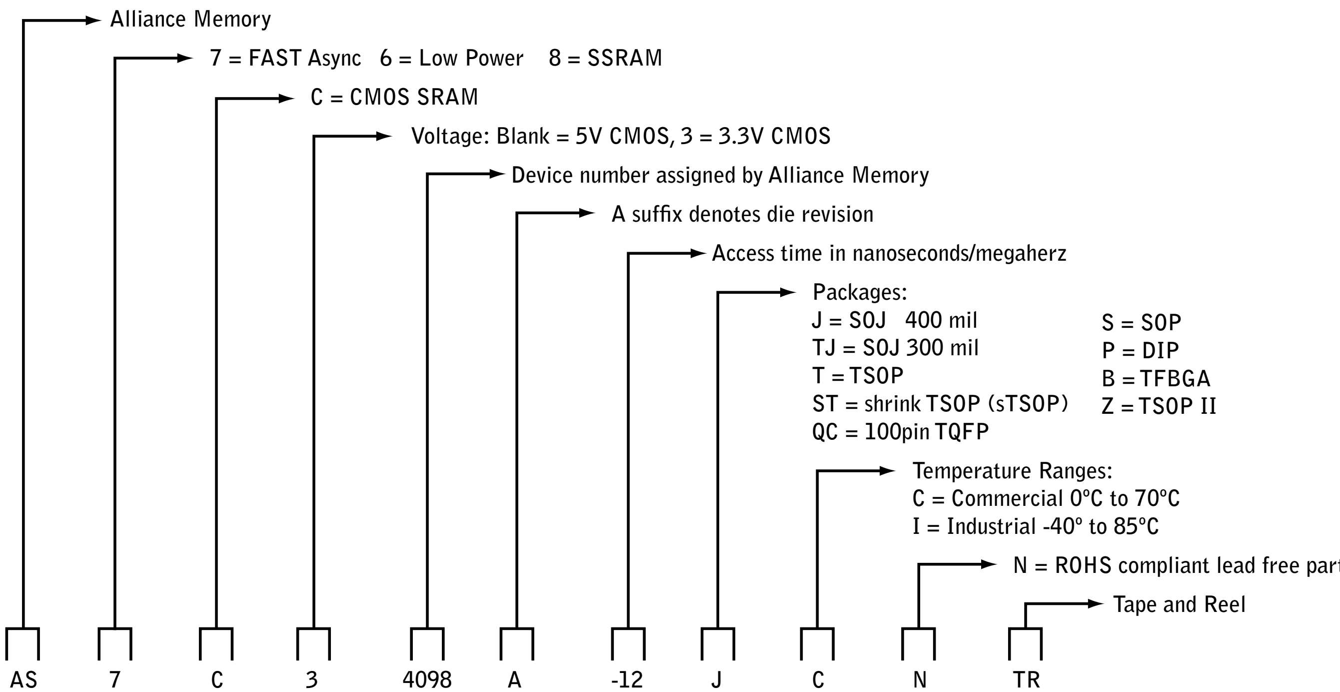
7 "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED NARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY

8 IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED

9 ALL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	JEDEC VARIATION			NOTE
	NOT YET REGISTERED			
	MIN	NOM	MAX	
A	—	—	1.20	
A1	.30	.35	.40	
A2	.78	85	.92	
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b	.35	.45	.50	5
CENTER BALL MATRIX	N/A			

Alliance Part numbering system



Ordering Information

Alliance	Organization	VCC Range	Operating Temp	Speed
AS8C803625	256K x 36	3.1 - 3.4V	Comercial 0 - 70C	7.5 ns
AS8C801825	512K x 18	3.1 - 3.4V	Comercial 0 - 70C	7.5 ns