

NTLJD3183CZ

Power MOSFET

20 V/–20 V, 4.7 A/–4.0 A, μ Cool™
Complementary, 2x2 mm, WDFN Package

Features

- WDFN 2x2 mm Package with Exposed Drain Pads for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ in 2x2 mm Package
- Footprint Same as SC–88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- ESD Protected
- This is a Pb–Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Load Switch
- Level Shift Circuits
- DC–DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain–to–Source Voltage		V_{DSS}	20	V	
Gate–to–Source Voltage		V_{GS}	± 8.0	V	
N–Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	3.8	A
			$T_A = 85^\circ\text{C}$	2.7	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	4.7		
P–Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	–3.2	A
			$T_A = 85^\circ\text{C}$	–2.3	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	–4.0		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.5	W
			$t \leq 5$ s	2.3	
N–Channel Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	2.6	A
		$T_A = 85^\circ\text{C}$	1.9		
P–Channel Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	–2.2	A
		$T_A = 85^\circ\text{C}$	–1.6		
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.71	W
Pulsed Drain Current	N–Ch	$t_p = 10$ μ s	I_{DM}	18	A
	P–Ch			–16	
Operating Junction and Storage Temperature		T_J, T_{STG}	–55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

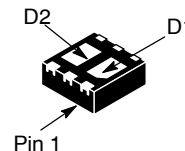
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.



ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
N–Channel 20 V	68 m Ω @ 4.5 V	4.7 A
	86 m Ω @ 2.5 V	4.2 A
	120 m Ω @ 1.8 V	3.5 A
P–Channel –20 V	100 m Ω @ –4.5 V	–4.0 A
	144 m Ω @ –2.5 V	–3.3 A
	200 m Ω @ –1.8 V	–2.8 A



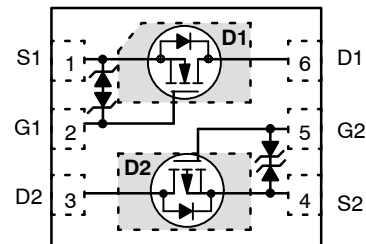
MARKING DIAGRAM

WDFN6
CASE 506AN



JN = Specific Device Code
M = Date Code
▪ = Pb–Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJD3183CZTAG	WDFN6 (Pb–Free)	3000/Tape & Reel
NTLJD3183CZTBG	WDFN6 (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJD3183CZ

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE OPERATION (SELF-HEATED)			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	
DUAL OPERATION (EQUALLY HEATED)			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0$ V	$I_D = 250$ μA	20		V
		P		$I_D = -250$ μA	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N	Ref to 25°C	$I_D = 250$ μA		15	mV/°C
		P		$I_D = -250$ μA		13	
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 25^\circ\text{C}$		1.0	μA
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-1.0	
		N	$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 85^\circ\text{C}$		10	
		P	$V_{GS} = 0$ V, $V_{DS} = -16$ V			-10	
Gate-to-Source Leakage Current	I_{GSS}	N	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 10	μA
		P				± 10	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250$ μA	0.4		1.0	V
		P		$I_D = -250$ μA	-0.4		-1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	N	Ref to 25°C	$I_D = 250$ μA		-3.0	mV/°C	
		P		$I_D = -250$ μA		2.0		
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5$ V, $I_D = 2.0$ A		34	68	m Ω	
		P	$V_{GS} = -4.5$ V, $I_D = -2.0$ A		68	100		
		N	$V_{GS} = 2.5$ V, $I_D = 2.0$ A		42	86		
		P	$V_{GS} = -2.5$ V, $I_D = -2.0$ A		90	144		
		N	$V_{GS} = 1.8$ V, $I_D = 1.7$ A		53	120		
		P	$V_{GS} = -1.8$ V, $I_D = -1.7$ A		125	200		
Forward Transconductance	g_{FS}	N	$V_{DS} = 5.0$ V, $I_D = 2.0$ A		7.0		S	
		P	$V_{DS} = -5.0$ V, $I_D = -2.0$ A		6.5			

NTLJD3183CZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit		
CHARGES, CAPACITANCES AND GATE RESISTANCE									
Input Capacitance	C_{ISS}	N	$f = 1.0 \text{ MHz}, V_{GS} = 0 \text{ V}$	$V_{DS} = 10 \text{ V}$		355	pF		
		P		$V_{DS} = -10 \text{ V}$		450			
Output Capacitance	C_{OSS}	N		$V_{DS} = 10 \text{ V}$		70			
		P		$V_{DS} = -10 \text{ V}$		90			
Reverse Transfer Capacitance	C_{RSS}	N		$V_{DS} = 10 \text{ V}$		50			
		P		$V_{DS} = -10 \text{ V}$		62			
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 3.8 \text{ A}$		4.6		7.0	nC
		P		$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.8 \text{ A}$		5.2		7.8	
Threshold Gate Charge	$Q_{G(TH)}$	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 3.8 \text{ A}$		0.3				
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.8 \text{ A}$		0.3				
Gate-to-Source Charge	Q_{GS}	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 3.8 \text{ A}$		0.6				
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.8 \text{ A}$		0.84				
Gate-to-Drain Charge	Q_{GD}	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}, I_D = 3.8 \text{ A}$		1.15				
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -3.8 \text{ A}$		1.5				

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5 \text{ V}, V_{DD} = 5 \text{ V}, I_D = 2.0 \text{ A}, R_G = 2.0 \Omega$		6.2		ns
Rise Time	t_r				5.5		
Turn-Off Delay Time	$t_{d(OFF)}$				15		
Fall Time	t_f				14		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5 \text{ V}, V_{DD} = -5 \text{ V}, I_D = -2.0 \text{ A}, R_G = 2.0 \Omega$		6.6		
Rise Time	t_r				9.0		
Turn-Off Delay Time	$t_{d(OFF)}$				14		
Fall Time	t_f				12.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	$I_S = 1.0 \text{ A}$		0.65	1.0	V	
		P		$I_S = -1.0 \text{ A}$		-0.73	-1.0		
		N	$V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$	$I_S = 1.0 \text{ A}$		0.55			
		P		$I_S = -1.0 \text{ A}$		-0.62			
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0 \text{ V}, dI_S / dt = 100 \text{ A}/\mu\text{s}$	$I_S = 1.0 \text{ A}$		21	ns		
		P		$I_S = -1.0 \text{ A}$		23			
Charge Time	t_a	N		$I_S = 1.0 \text{ A}$		10.5			
		P		$I_S = -1.0 \text{ A}$		13			
Discharge Time	t_b	N		$I_S = 1.0 \text{ A}$		10.5			
		P		$I_S = -1.0 \text{ A}$		10			
Reverse Recovery Charge	Q_{RR}	N		$I_S = 1.0 \text{ A}$		7.0			nC
		P		$I_S = -1.0 \text{ A}$		10			

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NTLJD3183CZ

N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

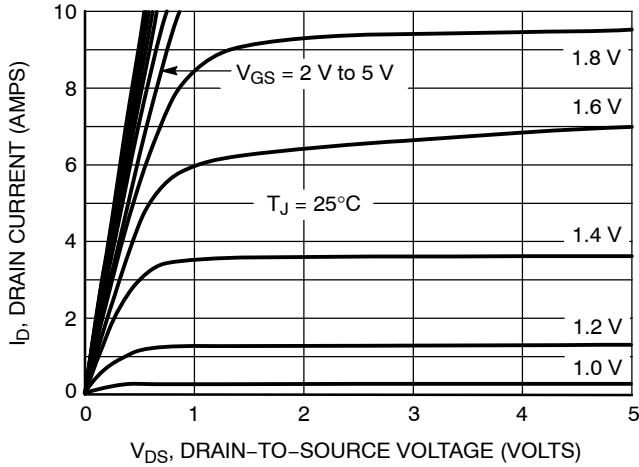


Figure 1. On-Region Characteristics

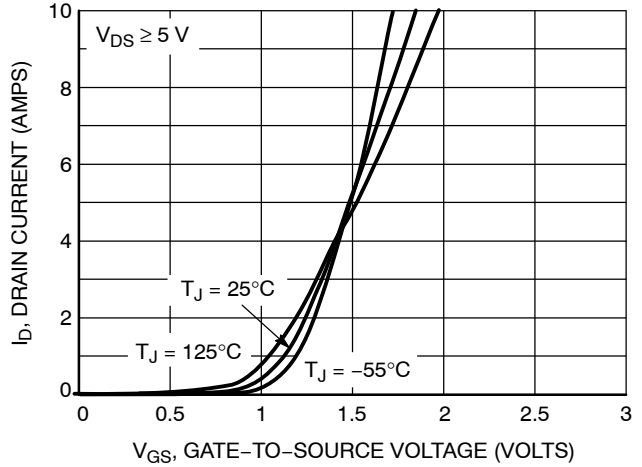


Figure 2. Transfer Characteristics

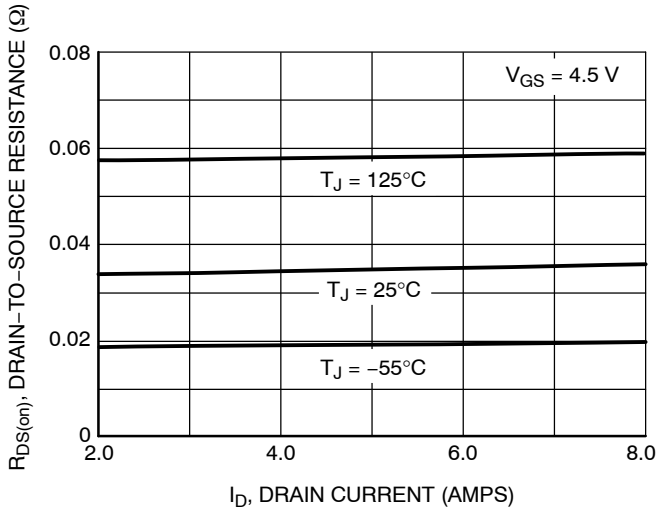


Figure 3. On-Resistance versus Drain Current

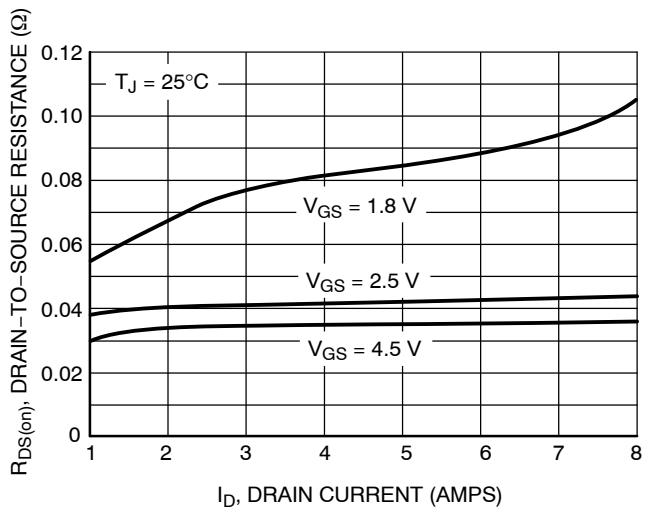


Figure 4. On-Resistance versus Drain Current and Gate Voltage

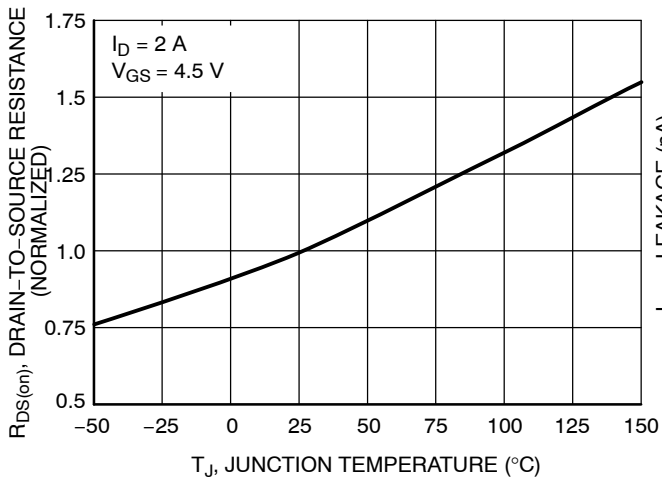


Figure 5. On-Resistance Variation with Temperature

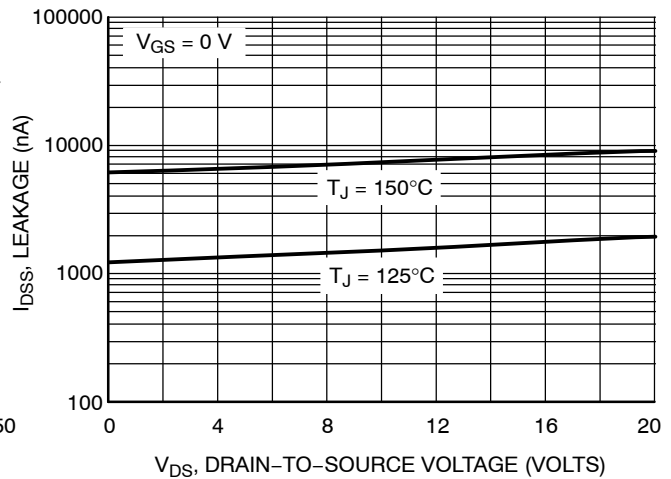


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTLJD3183CZ

N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

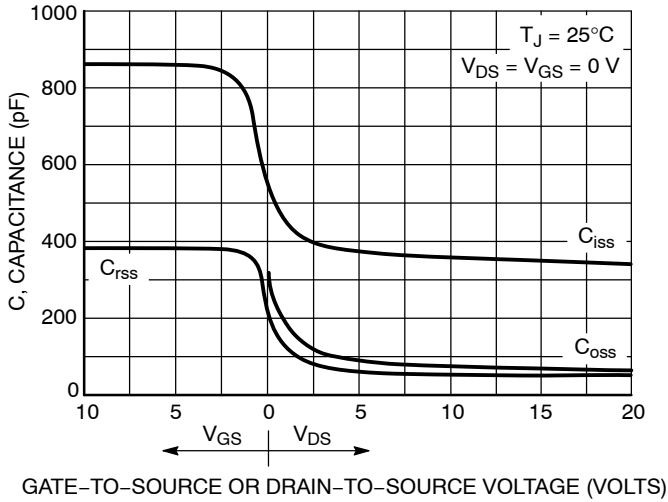


Figure 7. Capacitance Variation

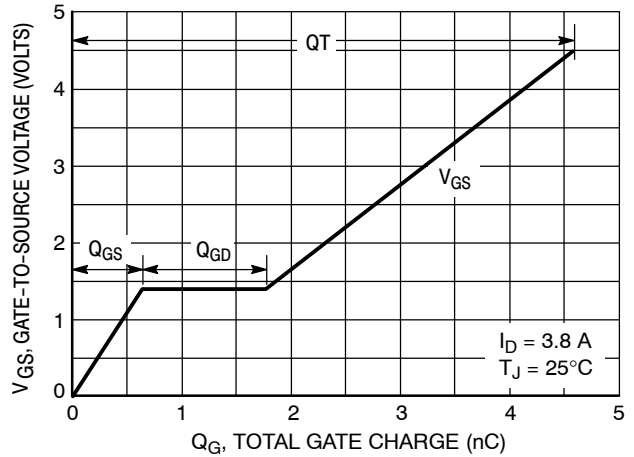


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

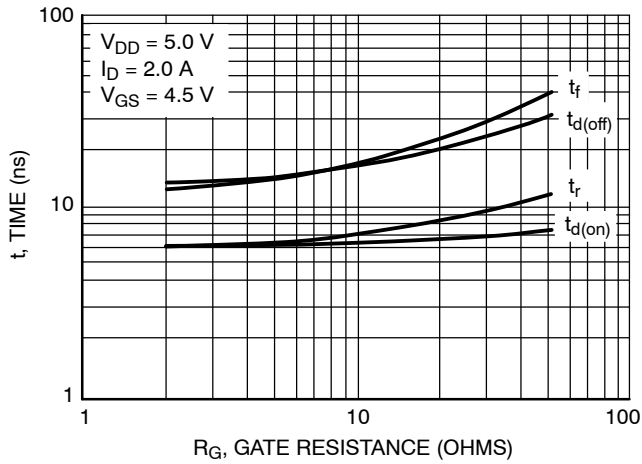


Figure 9. Resistive Switching Time Variation versus Gate Resistance

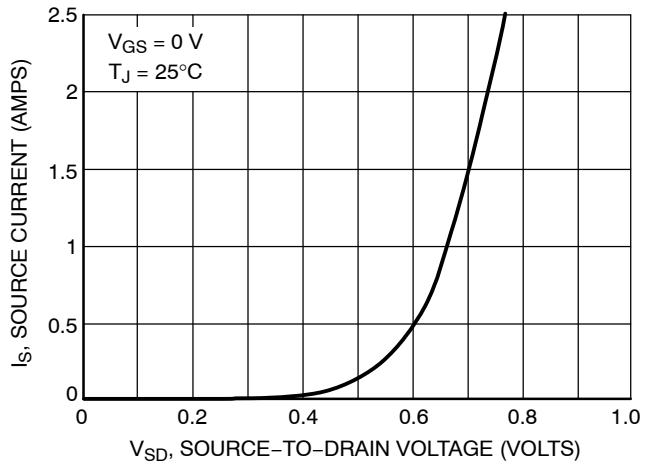


Figure 10. Diode Forward Voltage versus Current

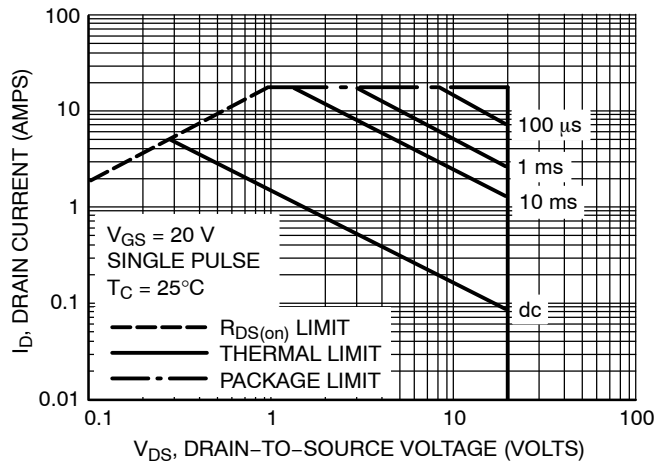


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTLJD3183CZ

P-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

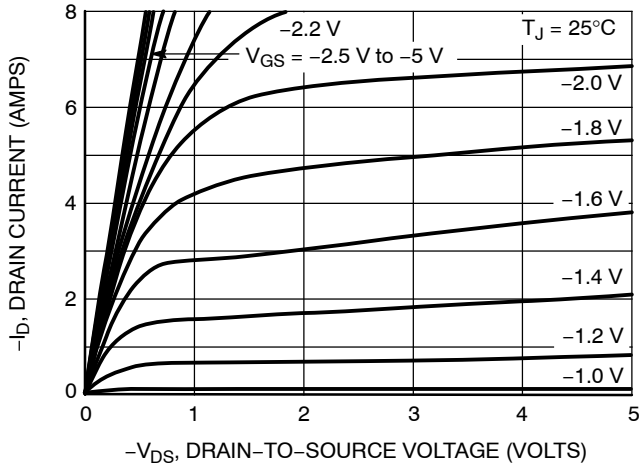


Figure 12. On-Region Characteristics

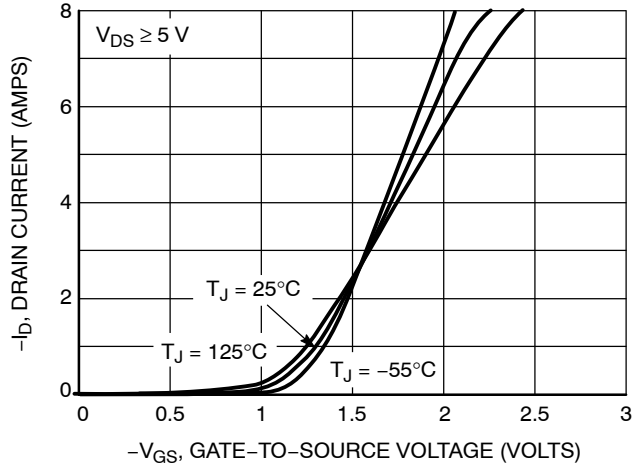


Figure 13. Transfer Characteristics

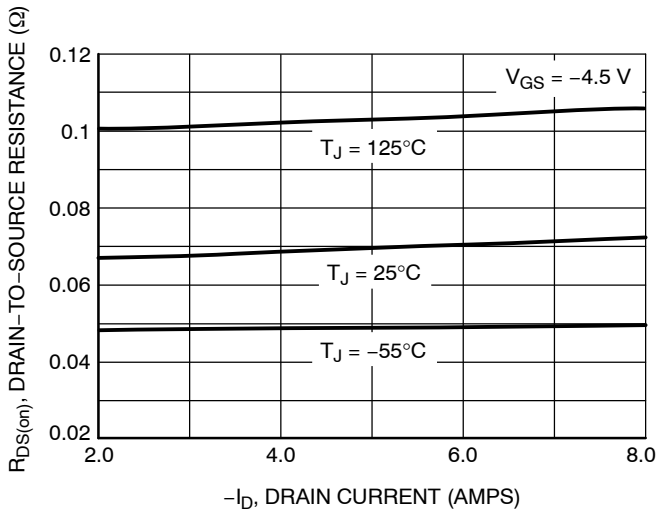


Figure 14. On-Resistance versus Drain Current

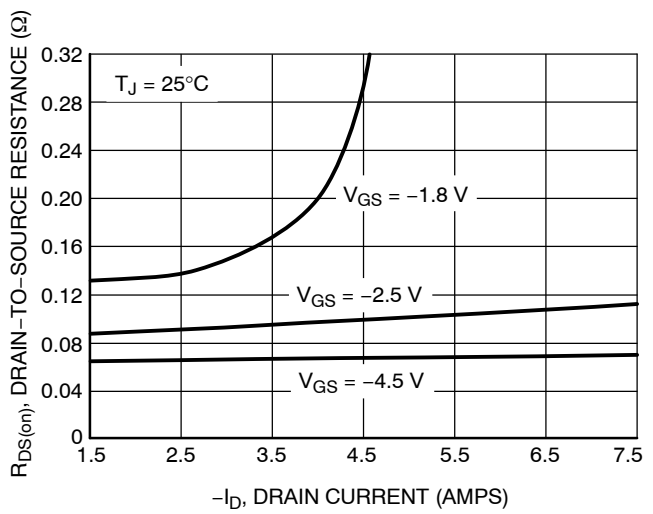


Figure 15. On-Resistance versus Drain Current and Gate Voltage

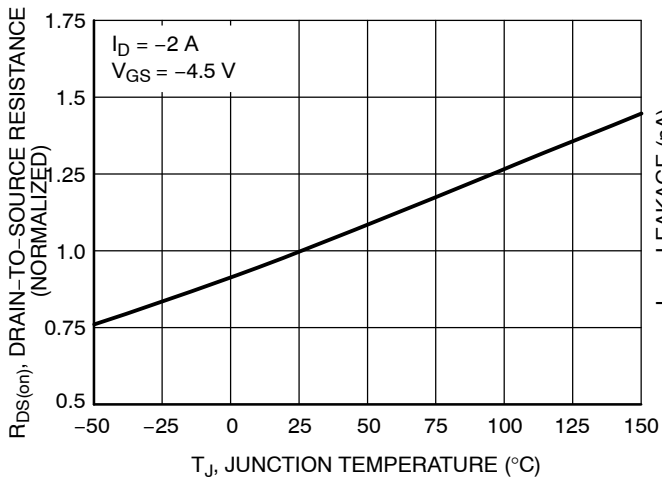


Figure 16. On-Resistance Variation with Temperature

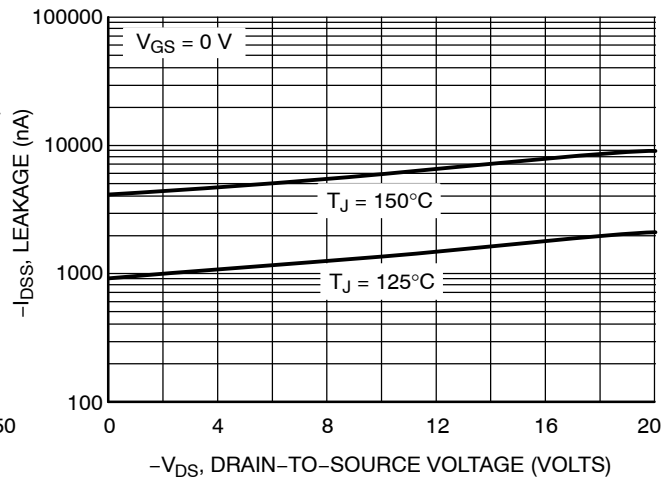


Figure 17. Drain-to-Source Leakage Current versus Voltage

NTLJD3183CZ

P-CHANNEL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

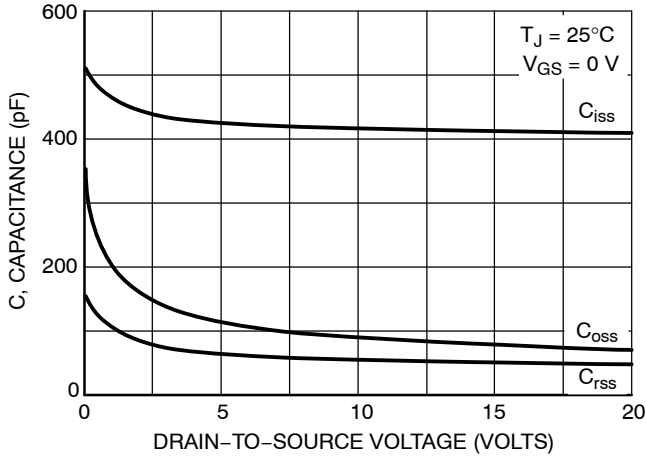


Figure 18. Capacitance Variation

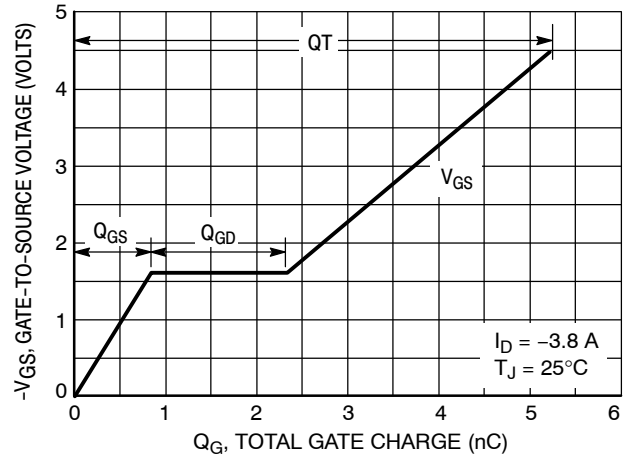


Figure 19. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

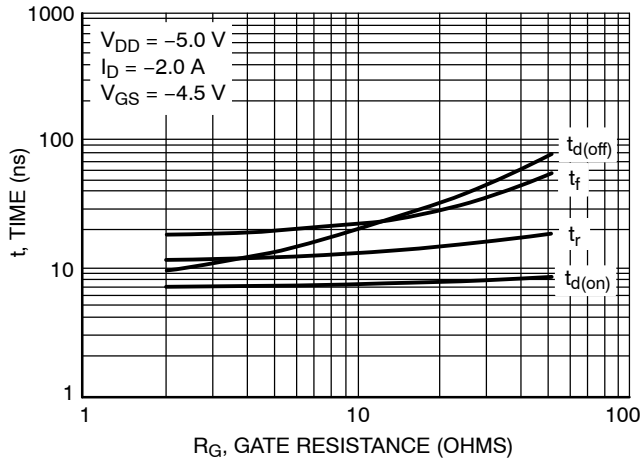


Figure 20. Resistive Switching Time Variation versus Gate Resistance

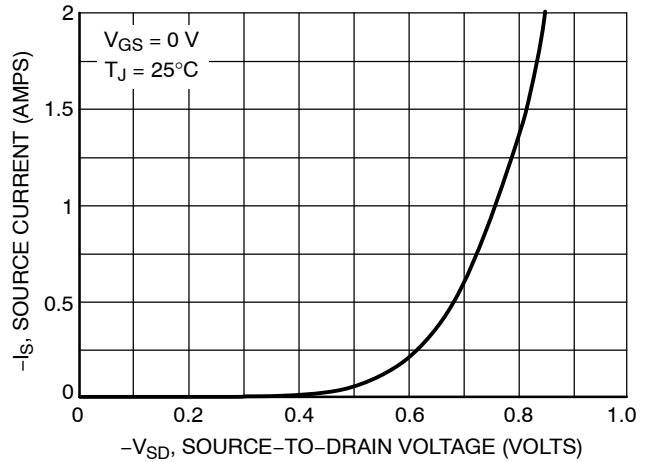


Figure 21. Diode Forward Voltage versus Current

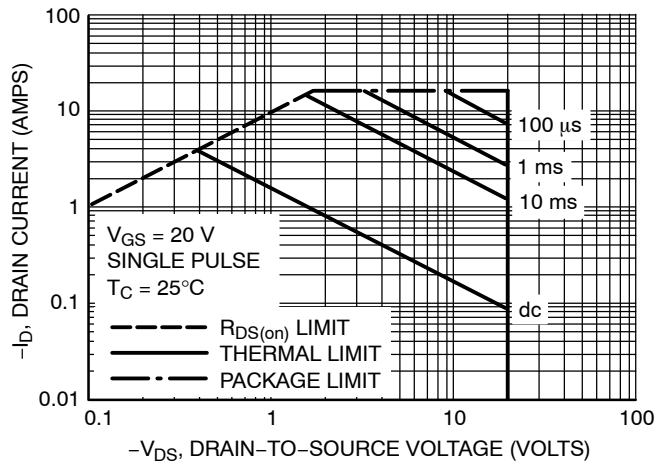


Figure 22. Maximum Rated Forward Biased Safe Operating Area

NTLJD3183CZ

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

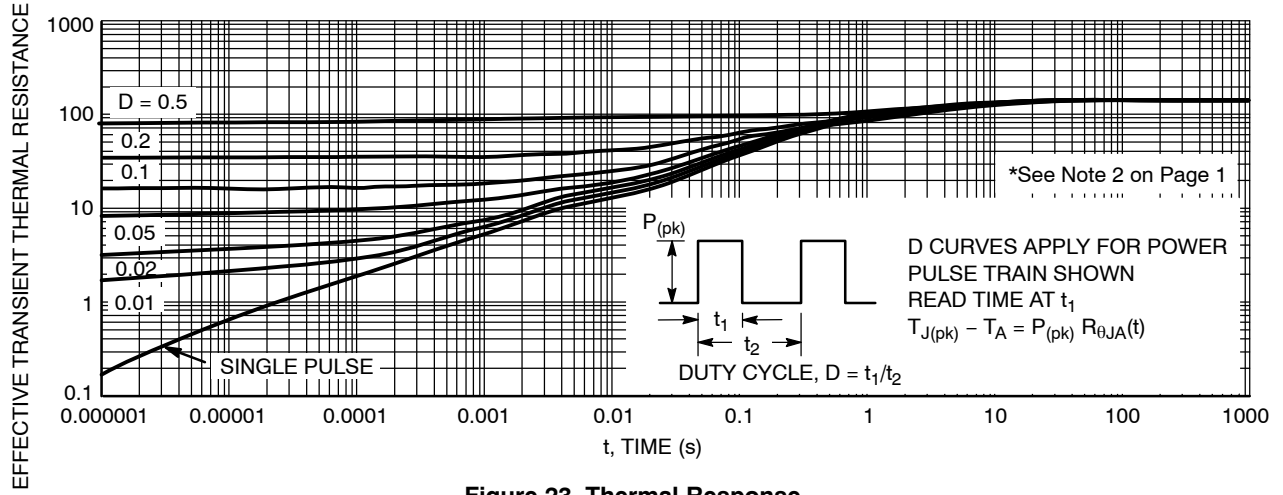
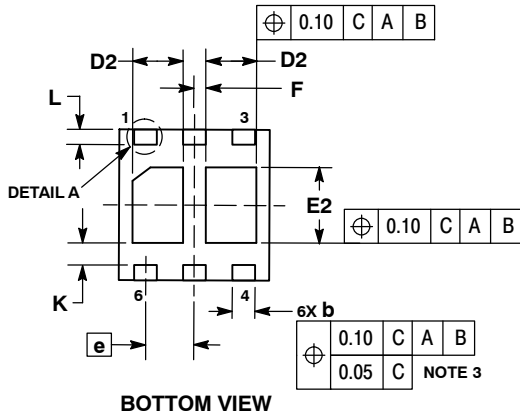
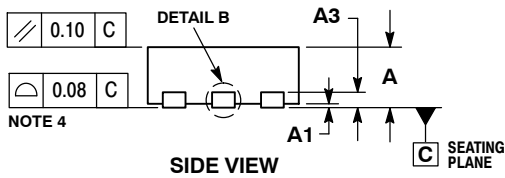
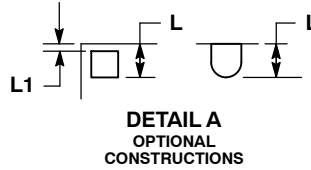
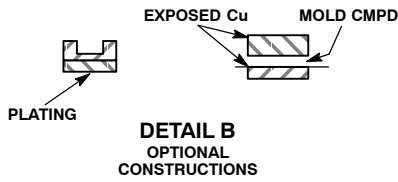
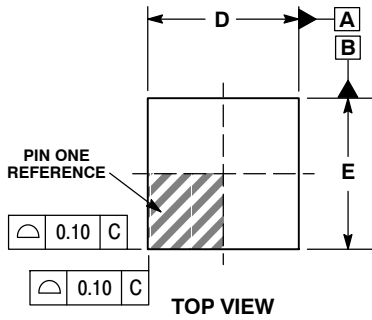


Figure 23. Thermal Response

NTLJD3183CZ

PACKAGE DIMENSIONS

WDFN6, 2x2
CASE 506AN-01
ISSUE D

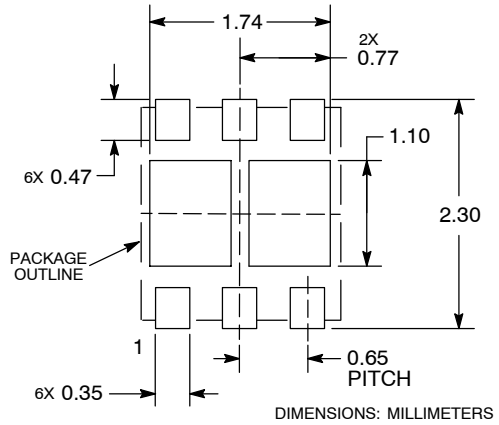


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.67
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

SOLDERMASK DEFINED MOUNTING FOOTPRINT



ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative