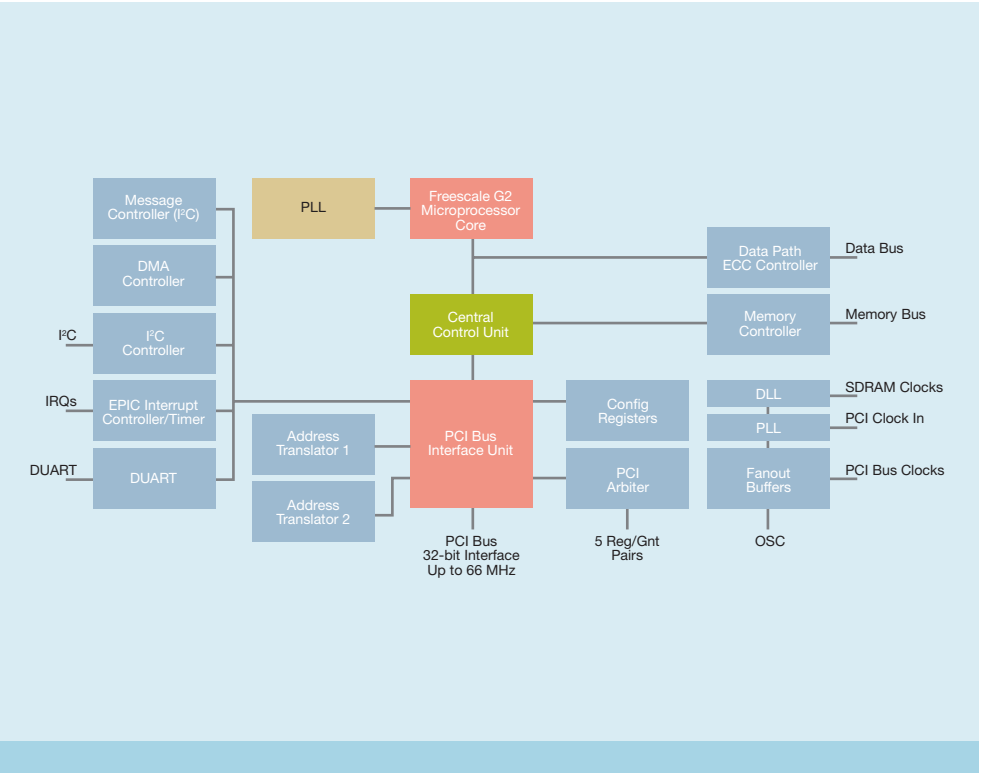
MPC8241 Host Processor Built on Power Architecture™ Technology

Overview

The MPC8241 integrated host processor implementing a core based on Power Architecture™ technology fits applications where cost, space, power consumption and performance are critical requirements. This device is designed to provide a high level of integration, reducing chip count from five discrete chips to one, thereby significantly reducing system component cost. High integration results in a simplified board design, low power consumption and a faster time to market solution. This cost-effective, general-purpose integrated processor targets systems using Peripheral Component Interconnect (PCI) interfaces in networking infrastructure, telecommunications and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications and image display systems.

MPC8241 Block Diagram



Product Highlights

- 166 MHz–266 MHz processor core
- 32-bit PCI interface operating at up to 66 MHz
- Memory controller offering SDRAM support up to 133 MHz operation, support up to 2 GB
- General-purpose I/O and ROM interface support
- Two-channel DMA controller that supports chaining
- Messaging unit with I_2O messaging support capability
- Industry-standard I^2C interface
- Programmable interrupt controller with multiple timers and counters
- 16550 compatible dual universal asynchronous receiver/transmitter (DUART)

Typical Applications

- Wireless LAN
- Routers/switches
- Embedded computing
- Multi-channel modems
- Network storage
- Image display systems
- Enterprise I/O processor
- Internet access device (IAD)
- Disk controller for RAID systems
- Copier/printer board control

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MPC8241 Integrated Host Processor	
CPU Speeds—Internal	166 MHz–266 MHz
CPU Bus Dividers	2.0, 2.5, 3.0, 4.0, 4.5
Memory Bus Dividers	1.0, 1.5, 2.0, 3.0
PCI Interface	32-bit (up to 66 MHz)
Memory Interface	64-bit (up to 100 MHz) + 8-bit parity
Instructions Per Clock	3 (2 + branch)
L1 Cache	16 KB instruction 16 KB data
Typical Power Dissipation (est.)	1.8 watts @ 266 MHz (with FPU on and @ 1.8V)
Package	357 PBGA
Process	0.25µ 5LM CMOS
Voltage	3.3V I/O, 1.8V internal
Dhrystone (2.1) MIPS	488 @ 266 MHz
603e Processor Core Functional Units	Integer, floating point unit, branch processing, load/store, PCI, DMA, memory control
Peripheral Logic Functional Units	I_2O, I^2C, EPIC, ATU, PCI and memory clocks, ECC controller x2 DUART

Technical Specifications

G2 Processor Core

- High-performance, superscalar processor core
- Floating point unit, integer, load/store, system register and branch processing unit
- 16 KB instruction cache, 16 KB data cache
- Lockable portion of L1 cache
- Dynamic power management
- Software-compatible with the Freescale processor families implementing Power Architecture technology

Power Architecture On-Chip Peripheral Logic/Memory Interface

- 133 MHz memory bus capability
- Programmable timing supporting SDRAM
- High-bandwidth bus (32-bit/64-bit data bus) to DRAM
- Supports one to eight banks of 16-, 64-, 128-, 256- or 512-bit SDRAM
- Supports 1 MB to 2 GB DRAM memory
- Contiguous memory mapping
- 272 MB of ROM space
- 8-, 16-, 32- or 64-bit ROM
- Supports bus-width writes to flash
- Read-modify-write parity support (selectable)
- ECC support (selectable)
- SDRAM, DRAM buffer data path
- Error injection/capture on data path
- Low voltage transistor transistor logic (LVTTL) compatible
- PortX: 8-, 16-, 32- or 64-bit general-purpose I/O port uses ROM controller interface with address strobe

32-bit PCI Interface Operating Up to 66 MHz

- PCI 2.2V compatible
- PCI 5.0V tolerant
- Support for PCI-locked accesses to memory
- Support for accesses to all PCI address spaces
- Selectable big- or little-endian operation
- Store gathering of processor-to-PCI writes and PCI-to-memory writes
- Memory prefetching of PCI read accesses
- Parity support (selectable)
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)

PCI Agent Mode Capability

- Dual address translation unit (ATU)
- Run time register access
- PCI configuration register access

Two-Channel Integrated DMA Controller

- Supports direct or chaining modes
- Scatter gather
- Interrupt on completed segment, chain and error
- Local to local memory
- PCI to PCI memory
- PCI to local memory
- Local to PCI memory
- Message unit
- Intelligent input/output message controller (I_2O)
  - Two door-bell registers
  - Inbound and outbound messaging registers
- Inter-integrated circuit controller (I^2C)
  - Full master/slave support
- Embedded programmable interrupt controller (EPIC)
- Five hardware interrupts (IRQs) or 16 serial interupts
- Four programmable timers

Integrated PCI Bus and SDRAM Clock Generation Programmable Memory and PCI Bus Drivers Debug Features

- Watchpoint monitor
- Memory attribute and PCI attribute signals
- JTAG/COP (common on-board processor) for in-circuit hardware debugging

Dual UART

Contact Information

Freescale offers user's manuals, application notes and sample code for all of its communications processors. Local support for these products is also provided. Information can be found at **www.freescale.com**.

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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