# LE4ASS21PEH

**16GB Unbuffered 2048Mx64 DDR4 SO-DIMM 1.2V** **Up to PC4-2133 CL 15-15-15**

## General Description

This Legacy device is a JEDEC standard unbuffered SO-DIMM module, based on CMOS DDR4 SDRAM technology, and is available as a 2048Mx64 (16GB). This device consists of 16 CMOS DDR4 SDRAMs in FBGA packages on a 260-pin glass epoxy substrate.

The memory array is designed with Double Data Rate (DDR4) Synchronous DRAMs for unbuffered applications. The pipelined, multibanked architecture of DDR4 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth. Decoupling capacitors are mounted on the PCB board in parallel for each DDR4 SDRAM, which provides proper voltage supply impedance over the whole frequency range of operations, in accordance with JEDEC specifications.

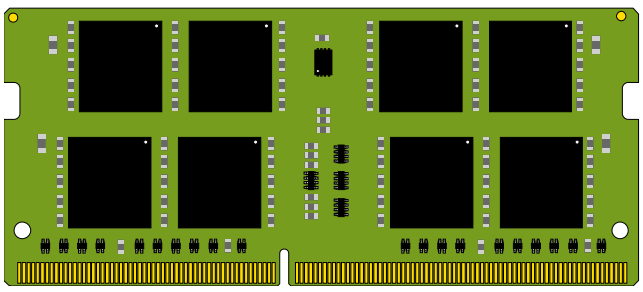
These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device, using the 2-pin I2C protocol. The first 383 bytes are programmed with configuration data and the second 127 bytes are available to the customer.

***Legacy Electronics offers a wide range of products featuring industry leading compatibility, manufactured to the highest quality standards and made entirely in America.***

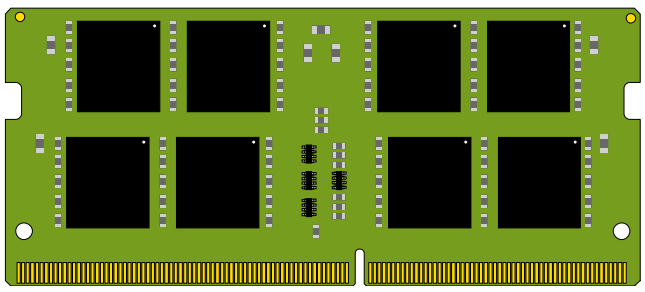
## Features

- 260-pin Unbuffered 8-Byte DDR4 SDRAM Memory Module for PC and Workstation main memory applications
- Assembled using: 1024Mx8 components
- Dual rank organization 2048Mx64
- JEDEC standard 1.2V I/O
- VDD = +1.2V ± 0.06V, VPP = +2.5V TYP
- 16 internal banks; 4 groups of 4 banks each
- RESET pin for improved system stability
- Differential clock inputs (CK, CK#)
- Multiplexed command and address bus
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register set
- Adjustable data output drive strength
- Terminated command, address, and control bus
- On-die $V_{REF}DQ$ generation and calibration
- TOPER operating Temperature –40°C ~ 85°C
- Serial Presence Detect (SPD) with EEPROM
- Impedance controlled 8-layer PCB Technology
- JEDEC standard form factor (69.6 mm x 30.0 mm)
- JEDEC DDR4 Raw Card E1
- RoHS Compliant

Front View



Back View



# Part Number and Timing Parameters

| Part Numbers | Modules Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL-tRCD-tRP) |
|---|---|---|---|---|---|
| LE4ASS21PEH-ME100-00100 | 16GB | 2048Mx64 | 17.0 GB/s | 0.93ns/2133 MT/s | 15-15-15 |
| All part numbers with a (-XXXXXX) Designate DRAM die revision and option codes | | | | | |

# Address Table

| Parameters | 16GB Density |
|---|---|
| Refresh Count | 8K |
| Row Addressing | 32K (A0 ~ A14) |
| Device Bank Addressing | 16 (BA0 ~ BA1)(BG0 ~ BG1) |
| Device Configuration | 8GB(1024Mx8) |
| Column Addressing | 1K (A0 ~ A9) |
| Module Rank Addressing | 2 (S0#, S1#) |

# Pin Assignments

| 260-Pin SO-DIMM Pins FRONT | | | | | | | | | 260-Pin SO-DIMM Pins BACK | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
| 1 | VSS | 67 | DQ29 | 133 | A1 | 199 | DM5/ DBI5# | | 2 | VSS | 68 | VSS | 134 | EVENT# (NC) | 200 | DQS5 |
| 3 | DQ5 | 69 | VSS | 135 | VDD | 201 | VSS | | 4 | DQ4 | 70 | DQ24 | 136 | VDD | 202 | VSS |
| 5 | VSS | 71 | DQ25 | 137 | CK0 | 203 | DQ46 | | 6 | VSS | 72 | VSS | 138 | CK1# | 204 | DQ47 |
| 7 | DQ1 | 73 | VSS | 139 | CK0# | 205 | VSS | | 8 | DQ0 | 74 | DQS3# | 140 | CK1 | 206 | VSS |
| 9 | VSS | 75 | DM3/DBI3 | 141 | VDD | 207 | DQ42 | | 10 | VSS | 76 | DQS3 | 142 | VDD | 208 | DQ43 |
| 11 | DQS0# | 77 | VSS | 143 | PARITY | 209 | VSS | | 12 | DM0/ DBI0# | 78 | VSS | 144 | A0 | 210 | VSS |
| 13 | DQS0 | 79 | DQ30 | 145 | BA1 | 211 | DQ52 | | 14 | VSS | 80 | DQ31 | 146 | A10/AP | 212 | DQ53 |
| 15 | VSS | 81 | VSS | 147 | VDD | 213 | VSS | | 16 | DQ6 | 82 | VSS | 148 | VDD | 214 | VSS |
| 17 | DQ7 | 83 | DQ26 | 149 | S0 | 215 | DQ49 | | 18 | VSS | 84 | DQ27 | 150 | BA0 | 216 | DQ48 |
| 19 | VSS | 85 | VSS | 151 | A14/WE# | 217 | VSS | | 20 | DQ2 | 86 | VSS | 152 | A16/RAS# | 218 | VSS |
| 21 | DQ3 | 87 | CB5 | 153 | VDD | 219 | DQS6# | | 22 | VSS | 88 | CB4 | 154 | VDD | 220 | DM6/ DBI6# |
| 23 | VSS | 89 | VSS | 155 | ODT0 | 221 | DQS6 | | 24 | DQ12 | 90 | VSS | 156 | A15/CAS# | 222 | VSS |
| 25 | DQ13 | 91 | CB1 | 157 | S1# | 223 | VSS | | 26 | VSS | 92 | CB0 | 158 | A13 | 224 | DQ54 |
| 27 | VSS | 93 | VSS | 159 | VDD | 225 | DQ55 | | 28 | DQ8 | 94 | VSS | 160 | VDD | 226 | VSS |
| 29 | DQ9 | 95 | DQS8# | 161 | ODT1 | 227 | VSS | | 30 | VSS | 96 | NC (DBI8#) | 162 | C0 S2# (NC) | 228 | DQ50 |
| 31 | VSS | 97 | DQS8 | 163 | VDD | 229 | DQ51 | | 32 | DQS1# | 98 | VSS | 164 | VREFCA | 230 | VSS |
| 33 | DM1/DBI1 | 99 | VSS | 165 | C1 S3# (NC) | 231 | VSS | | 34 | DQS1 | 100 | CB6 | 166 | SA2 | 232 | DQ60 |
| 35 | VSS | 101 | CB2 | 167 | VSS | 233 | DQ61 | | 36 | VSS | 102 | VSS | 168 | VSS | 234 | VSS |
| 37 | DQ15 | 103 | VSS | 169 | DQ37 | 235 | VSS | | 38 | DQ14 | 104 | CB7 | 170 | DQ36 | 236 | DQ57 |
| 39 | VSS | 105 | CB3 | 171 | VSS | 237 | DQ56 | | 40 | VSS | 106 | VSS | 172 | VSS | 238 | VSS |
| 41 | DQ10 | 107 | VSS | 173 | DQ33 | 239 | VSS | | 42 | DQ11 | 108 | RESET# | 174 | DQ32 | 240 | DQS7# |
| 43 | VSS | 109 | CKE0 | 175 | VSS | 241 | DM7/ DBI7# | | 44 | VSS | 110 | CKE1 | 176 | VSS | 242 | DQS7 |
| 45 | DQ21 | 111 | VDD | 177 | DQS4# | 243 | VSS | | 46 | DQ20 | 112 | VDD | 178 | DM4/ DBI4# | 244 | VSS |
| 47 | VSS | 113 | BG1 | 179 | DQS4 | 245 | DQ62 | | 48 | VSS | 114 | ACT# | 180 | VSS | 246 | DQ63 |
| 49 | DQ17 | 115 | BG0 | 181 | VSS | 247 | VSS | | 50 | DQ16 | 116 | ALERT# | 182 | DQ39 | 248 | VSS |
| 51 | VSS | 117 | VDD | 183 | DQ38 | 249 | DQ58 | | 52 | VSS | 118 | VDD | 184 | VSS | 250 | DQ59 |
| 53 | DQS2# | 119 | A12 | 185 | VSS | 251 | VSS | | 54 | DM2/ DBI2# | 120 | A11 | 186 | DQ35 | 252 | VSS |
| 55 | DQS2 | 121 | A9 | 187 | DQ34 | 253 | SCL | | 56 | VSS | 122 | A7 | 188 | VSS | 254 | SDA |
| 57 | VSS | 123 | VDD | 189 | VSS | 255 | VDDSPD | | 58 | DQ22 | 124 | VDD | 190 | DQ45 | 256 | SA0 |
| 59 | DQ23 | 125 | A8 | 191 | DQ44 | 257 | VPP | | 60 | VSS | 126 | A5 | 192 | VSS | 258 | VTT |
| 61 | VSS | 127 | A6 | 193 | VSS | 259 | VPP | | 62 | DQ18 | 128 | A4 | 194 | DQ41 | 260 | SA1 |
| 63 | DQ19 | 129 | VDD | 195 | DQ40 | - | - | | 64 | VSS | 130 | VDD | 196 | VSS | - | - |
| 65 | VSS | 131 | A3 | 197 | VSS | - | - | | 66 | DQ28 | 132 | A2 | 198 | DQS5# | - | - |

# Pin Descriptions

| SYMBOL | TYPE | FUNCTION |
|---|---|---|
| CK0 ~ CK0#<br>CK1 ~ CK1# | Input | **Clock:** CK, CK# are differential clock inputs. All the DDR4 SDRAM address and control inputs are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (read) data is reference to the crossing of CK and CK# (Both directions of crossing). |
| CKE0, CKE1 | Input | **Clock Enable:** Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. |
| S0#, | Input | **Chip Select:** Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks. |
| RAS#, CAS#, WE# | Input | **Command Inputs:** RAS#, CAS#, and WE# (S# as well) define the command being entered. |
| RESET# | Input | **Reset:** An active LOW CMOS input referenced to VSS and not referenced to VREFCA or VREFDQ. The reset pin input receiver is a CMOS input and is defined as a rail-to-rail signal with a DC HIGH ≥ 0.8 x VDDQ and DC LOW ≤ 0.2 x VDDQ (1.20V for HIGH and 0.30V for LOW). RESET# assertion and desertion are asynchronous. System applications will most likely be unterminated, heavily loaded, and have very slow slew rates. A slow slew rate receiver design is recommended along with implementing on-chip noise filtering to prevent false triggering (RESET# assertion minimum pulse width is 100ns). |
| ODT0 ~ ODT1 | Input | **On-Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command. |
| BA0 ~ BA1 | Input | **Bank Address:** BA0, BA1, and BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied. |
| A0 ~ A17 | Input | **Address Inputs:** During a Bank Activate command cycle, Address input defines the row address (RA0 ~ RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke auto precharge operation at the end of the burst read or write cycle. If AP is high, auto precharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto precharge is disabled. During a precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped). |
| ACT# | Input | **Activation Command Input:** ACT_n defines the Activation command being entered along with CS#. The input into RAS#/A16, CAS#/A15 and WE#/A14 will be considered as Row Address A16, A15 and A14. |
| A10 / AP | Input | **Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC# | Input | **Burst Chop:** A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| BG0, BG1 | Input | **Bank Group Inputs:** BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0. |
| DQS0 ~ DQS17<br>DQS0# ~DQS17# | Input / Output | **Data Strobe:** Output with READ data, input with WRITE data. DQS is edge-aligned with READ data and is centered in WRITE data. Used to capture data. |
| DQ0 ~ DQ63 | Input / Output | **Data I/Os:** Bidirectional Data bus. |
| ALERT# | Output | **Alert:** It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT# goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. |

# Pin Descriptions

| SYMBOL | TYPE | FUNCTION |
|---|---|---|
| Parity | Input | **Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT#, RAS#/A16, CAS#/A15, WE#/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS# LOW |
| ZQ | Supply | Reference Pin for ZQ calibration |
| $V_{DD}$ | Supply | **Power supply:** +1.5V (±0.075V) or 1.35V (1.283V to 1.45V) for low voltage modules. |
| $V_{TT}$ | Supply | **Termination Voltage:** Used for address, command, control, and clock nets. $V_{DD}$ /2 |
| $V_{DDSPD}$ | Supply | **Power supply:** Serial EEPROM positive power supply, 3.3V (3.0V to 3.6V). |
| $V_{REF}$DQ | Supply | **Reference Voltage:** DQ and DM. $V_{DD}$ /2 |
| $V_{REF}$CA | Supply | **Reference Voltage:** Command, address, and control. $V_{DD}$ /2 |
| $V_{SS}$ | Supply | **Ground.** |
| SDA | Input / Output | **Serial Presence-Detect Data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| SCL | Input / Output | **SCL Input Serial Clock for Presence-Detect:** SCL is used to synchronize the presence-detect data transfer to and from the module. |
| SA0 ~ SA2 | Input | **SA0 ~ SA2 Input SPD Address Inputs:** These pins are used to configure the presence-detect device. |
| NC | - | **No Connect:** These pins should be left unconnected. |
| RFU | - | **Reserved for future use:** No on DIMM electrical connection is present |

# Absolute Maximum DC Ratings

| Parameters[1] | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$ , $V_{OUT}$ | -0.4 | 1.5 | V |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 | 1.5 | V |
| Voltage on $V_{DD}Q$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 | 1.5 | V |
| Storage Temperature | $T_{STG}$ | -55 | 100 | °C |

[1] Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# Operating Temperature Range

| Parameters | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|
| DIMM Module Operating Temperature Range (ambient) | $T_{OPR}$[1] | -40 | 85 | °C |
| DRAM Component Case Temperature Range | $T_{OPR}$[1] | -25 | 95 | °C |

[1] Operating Temperature $T_{OPR}$ is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

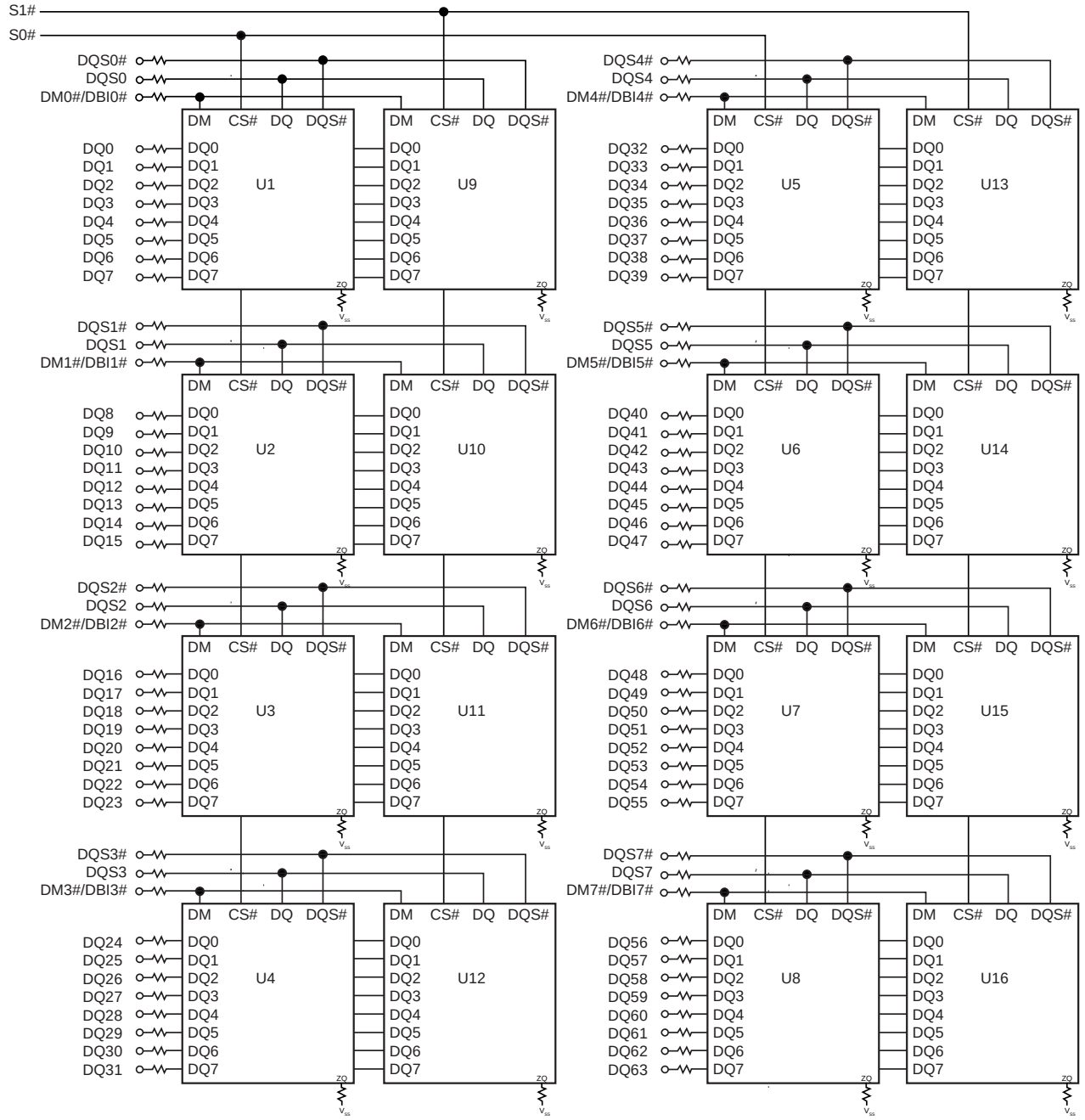
[2] The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 ± 70°C under all operating conditions. For Industrial Temperature DRAM case temperature must be maintained between -25 ± 95°C under all operating conditions.

# AC & DC Operating Conditions

| Parameters | Symbol | MIN | NOM | MAX |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.14 V | 1.2 V | 1.26 V |
| DRAM activating power supply | $V_{PP}$ | 2.375 V | 2.5 V | 2.75 V |
| I/O Supply Voltage[1] | $V_{DDQ}$ | 1.14 V | 1.2 V | 1.26 V |
| SPD Supply Voltage | $V_{DDSPD}$ | 2.5 V | 3.3 V | - |

[1] Under all conditions VDDQ must be less than or equal to VDD.

# Functional Block Diagram

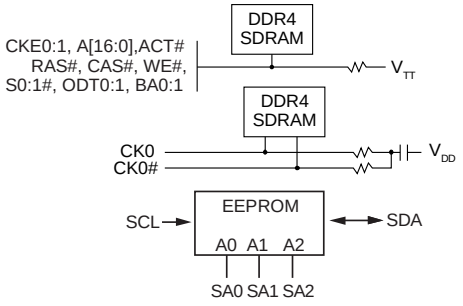



BA0-BA1 → BA0-BA1: DDR4 SDRAMs
A0-A16 → A0-A16: DDR4 SDRAMs
RAS# → RAS#: DDR4 SDRAMs
CAS# → CAS#: DDR4 SDRAMs
WE# → WE#: DDR4 SDRAMs
RESET# → RESET#: DDR4 SDRAMs
ALERT# → ALERT#: DDR4 SDRAMs
ACT# → ACT#: DDR4 SDRAMs
PARITY → PARITY: DDR4 SDRAMs
BG0-BG1 → BG0-BG1: DDR4 SDRAMs
CKE0 → CKE0: DDR4 SDRAMs
ODT0 → ODT0: DDR4 SDRAMs

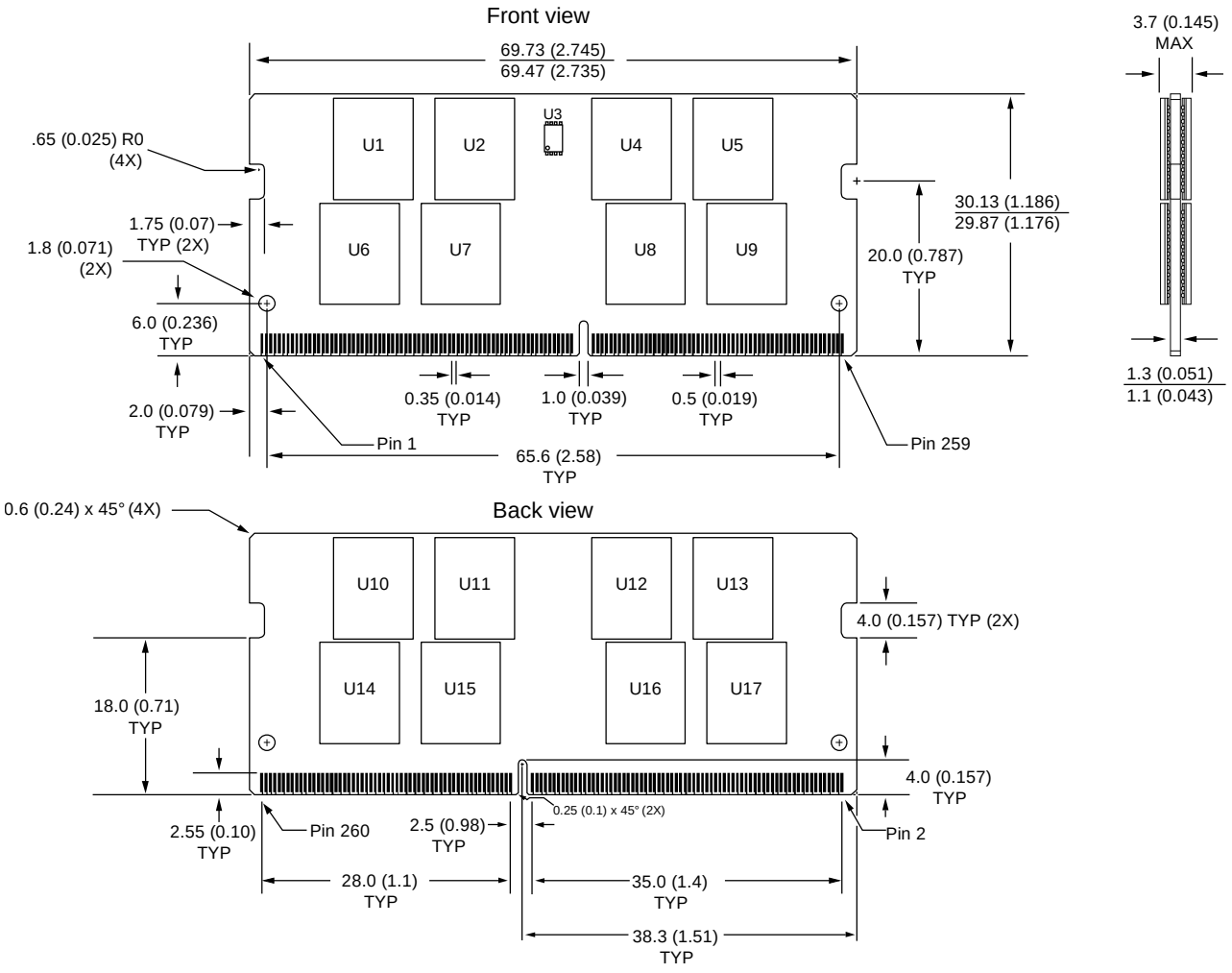
CK0, CK0# → DDR4 SDRAMs
CK1, CK1# → DDR4 SDRAMs

$V_{DDSPD}$ → SPD EEPROM
$V_{DD}$ → DDR4 SDRAMs
$V_{TT}$ → Cmd,Cntl,Add,Term
$V_{PP}$ → DDR4 SDRAMs
$V_{REF}CA$ → DDR4 SDRAMs
$V_{SS}$ → DDR4 SDRAMs

Address, command, control, and clock line terminations:



# Module Dimensions



# About Us

Located in Canton, South Dakota, Legacy Electronics specializes in designing and manufacturing a full line of high-density memory modules, printed circuit boards, SSDs, and other computer products.

Legacy Electronics is home of the patented Canopy® chip-stacking alternative, a three-dimensional printed circuit board subassembly and process technology. Legacy utilizes an ISO 9001:2008 certified Quality Management System.

Legacy's cutting edge products are available in a variety of densities, speeds, and voltage levels. Our standard and custom modules are available in a wide array of form factors, including JEDEC-standard DIMMs and SO-DIMMs. Our products exceed industry standards. All Legacy products are proudly made in the USA..

## Advanced tested memory products

Legacy Electronics is the only company to have a 100% pass rate for over 300 tests in a calendar year at CMTL (Computer Memory Test Labs).

In addition, CMTL awarded Legacy Electronics with a lifetime achievement award after 15 plus years of service with CMTL.

The CMTL Memory Module Certification Program performs advanced compatibility testing on motherboards from the industry's leading manufacturers like Intel®. All the modules listed at CMTL have passed rigorous cross platform certification testing criteria and are proven to be compatible with the motherboards on which they were tested.


## Contact Us

Give us a call or visit us online for more information about our products and services.

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