# Si5100/Si5110-EVB

## Evaluation Board Set for Si5100 and Si5110 OC-48/STM-16 SONET/SDH TRANSCEIVERS

### Description

The Si5100-EVB and Si5110-EVB motherboard/daughter card sets provide a platform for testing and characterizing Silicon Laboratories' Si5100/Si5110 SiPHY™ OC-48/STM-16 SONET/SDH Transceiver. The Si5100 and Si5110 transceiver devices provide full-duplex operation at serial data rates up to 2.7 Gbps. The transceiver device is mounted on the EVB daughter card. The high-speed serial signals are accessed via SMA connectors on the daughter card itself. The low-speed parallel data channels are routed from the daughter card to the motherboard through the industry-standard 300-pin meg-array connector.

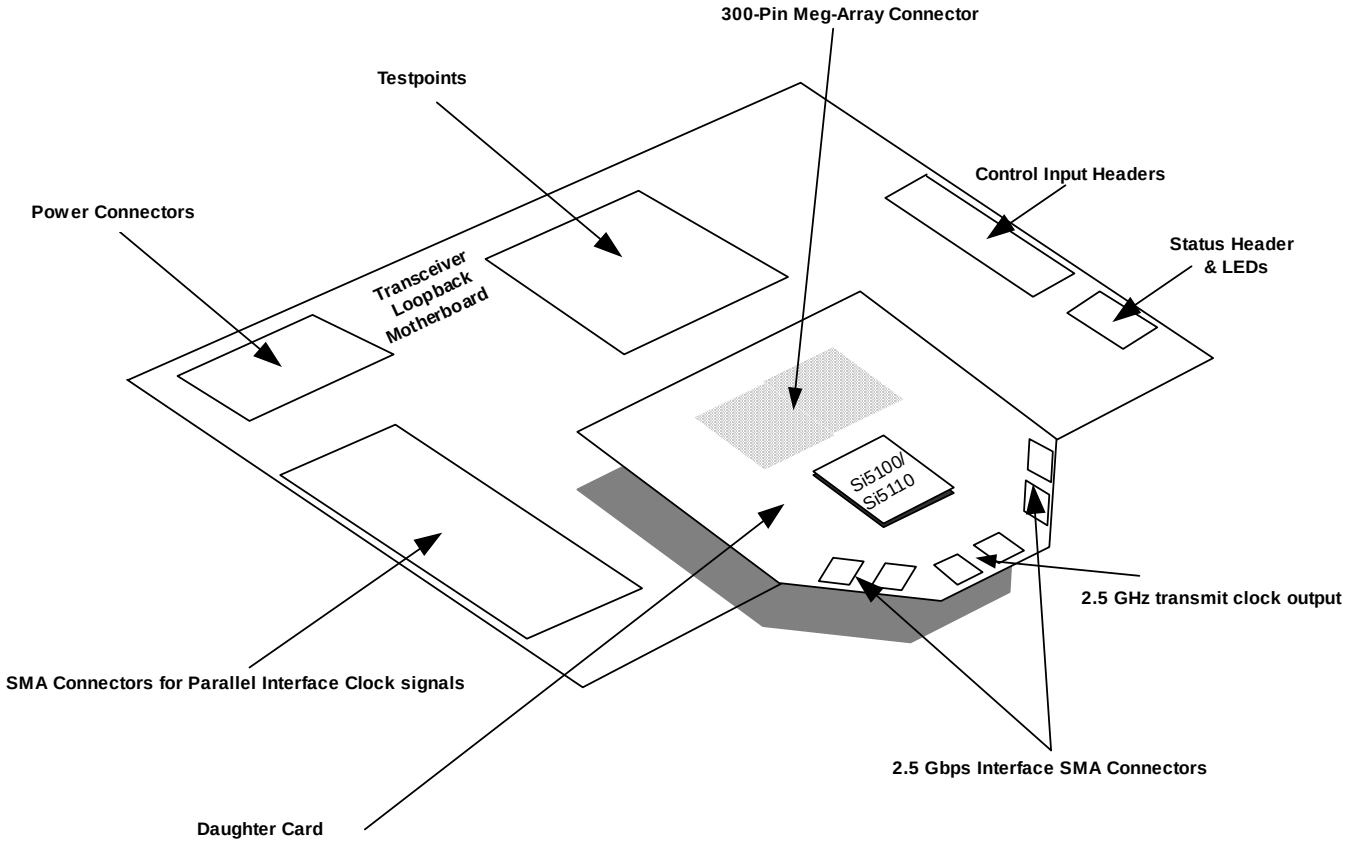
The included transceiver loopback motherboard provides a hardware connection between the transceiver low-speed parallel data outputs, RXDOUT, and the transceiver low-speed parallel data inputs, TXDIN. Test points are provided on the motherboard to allow monitoring of the parallel data channels. The clock signals associated with the low-speed data channels are routed to SMA connectors on the loopback motherboard. Static control and status signals are routed to standard 100-mil center posts.

An optional full-duplex motherboard is also available for the transceiver daughter card. The full-duplex motherboard also utilizes the industry-standard 300-pin meg-array connector to allow attachment of the daughter card. The full-duplex motherboard routes all of the transceiver low-speed parallel data outputs and inputs to standard SMA connectors. The optional full-duplex motherboard is useful when connecting the transceiver device to a parallel bit error rate tester (ParBERT), or in other applications that require full access to the low-speed parallel data channels.

### Features

- Separate supply connections for VDD (1.8 V) and VDDIO (1.8 V or 3.3 V) allow LVTTL I/Os to be powered at either 1.8 V or 3.3 V.
- Control inputs are jumper configurable.
- Status outputs brought out to headers for easy access.
- Potentiometers provided for controlling analog inputs.
- Loopback Motherboard (included) provides hardware path between low-speed parallel data outputs RXDOUT and low-speed parallel data inputs TXDIN.
- Optional full-duplex motherboard provides access to all low-speed parallel data outputs and inputs via SMA connectors.

## Motherboard/Daughter Card Set



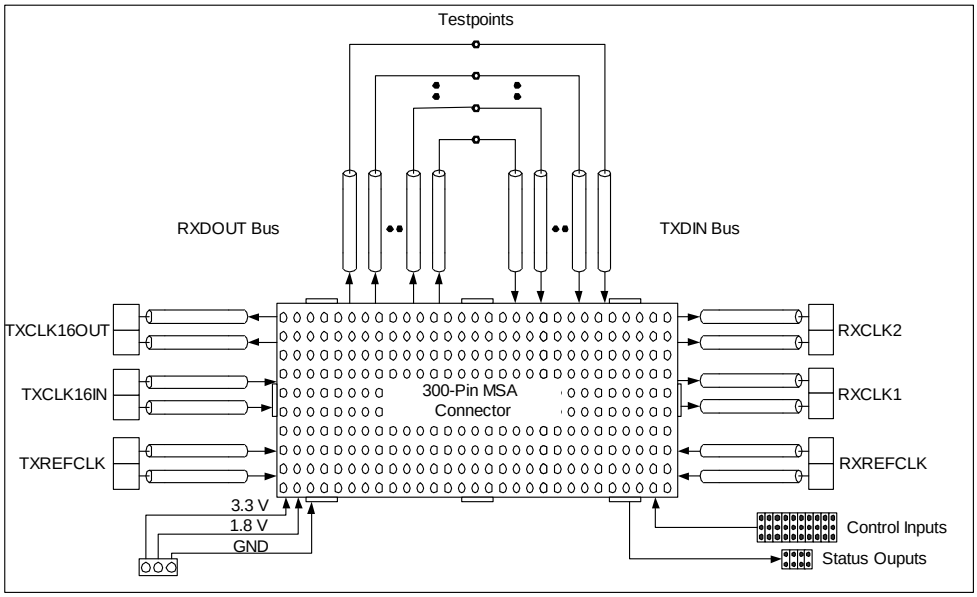



**Figure 1. Loopback Motherboard Functional Block Diagram**

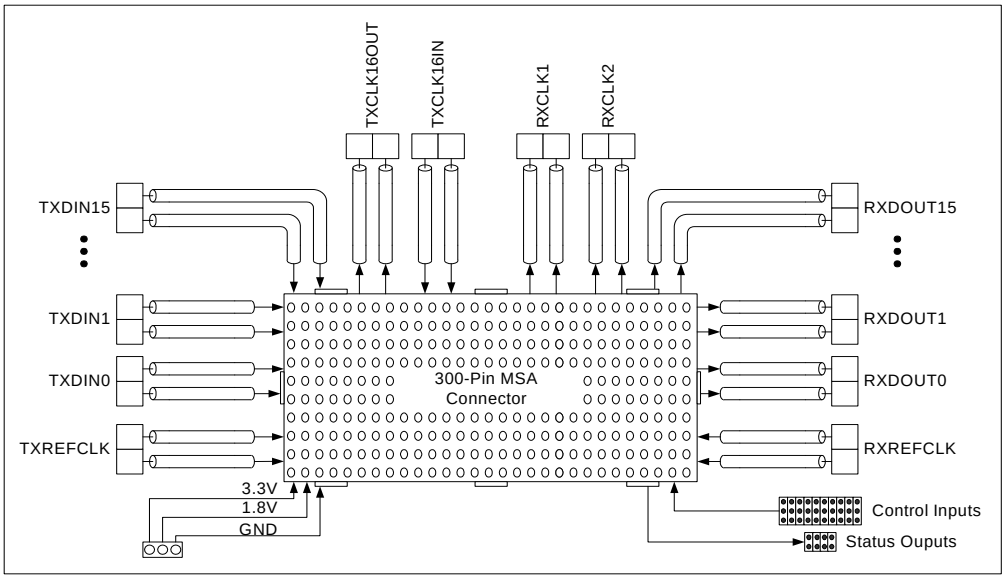



**Figure 2. Optional Full-Duplex Motherboard Functional Block Diagram**

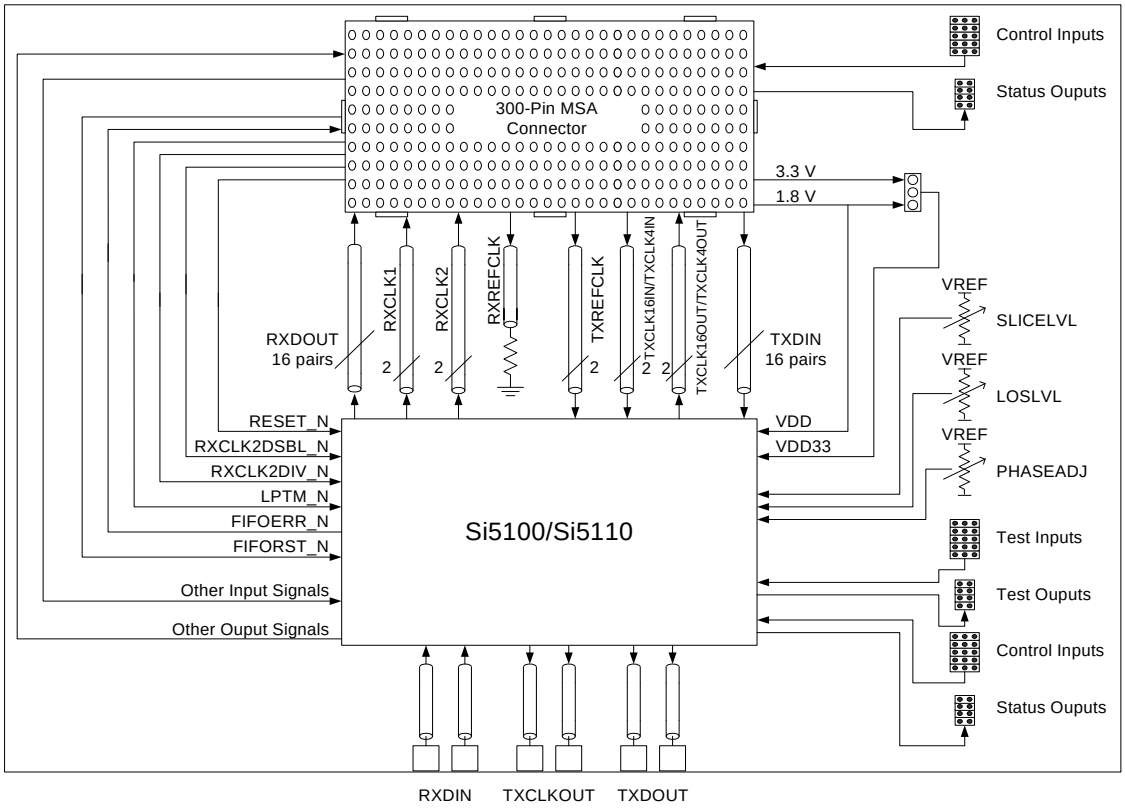



**Figure 3. Daughter Card Functional Block Diagram**

## Functional Description

The Si5100-EVB and Si5110-EVB motherboard and daughter card sets simplify characterization of the OC-48/STM-16 and FEC transceiver devices by providing convenient access to the device I/Os. Device performance can be evaluated in various modes by following the “Basic Test Setup” section.

## Power Supply

The transceiver device can be powered from a single 1.8 V supply or seperate 1.8 V and 3.3 V supplies. When the additional 3.3 V supply is applied, the status outputs are LVTTL compatible. The daughter card can be configured for either mode of operation by setting the VDD_IO SEL jumper as shown in Figure 4.

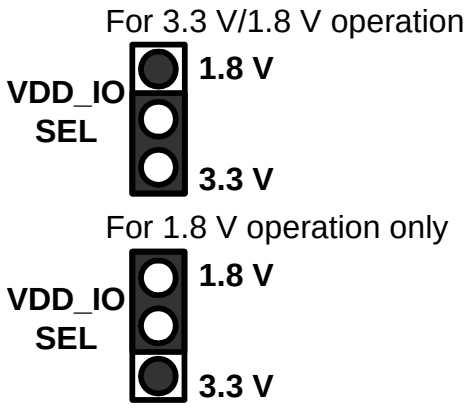



**Figure 4. VDD_IO Selection Jumpers**

## Control Inputs

The device control inputs are located on the motherboard and daughter card. Signals with equivalent module functions are routed to the motherboard header, JP1. Signals specific to the transceiver are routed on the daughter card to jumpers JP1 and JP2. In both cases, the signal is routed to the center pin of a three pin group where the adjacent pins are power and ground. The device inputs are pulled high or low so that leaving a signal unconnected will not harm the device.

## Status Outputs

The device status outputs are located on the motherboard and daughter card. Signals with equivalent module functions are routed to the motherboard header, JP2. Signals specific to the transceiver are routed on the daughter card to headers JP3 and JP4. In both cases, the signal is routed to a header pin adjacent to a ground pin.

## Data I/O Signals

The serial 2.5 Gbps data and 2.5 GHz clock paths are routed as coplanar differentially-coupled microstrip transmission lines on the daughter card. These three signals (RXDIN, TXCLKOUT, and TXDOUT) are ac coupled to standard SMA jacks for ease in connection to industry standard test equipment. Take care when connecting cables to these jacks. Use a standard SMA torque wrench to minimize reflections at the cable-to-jack interface. Finally, match all differential connections in length to minimize phase differences between the positive and negative terminals.

## Differential Parallel Data and Clock I/O Signals

The differential parallel data lines are routed through the 300-pin meg-array connector to the motherboard. The standard loopback motherboard directly couples the RXDOUT bus to the TXDIN bus. The optional full-duplex motherboard directly couples the RXDOUT and TXDIN buses to standard SMA jacks for connection to industry standard test equipment.

## Slice Level, Loss-of-Signal Level, and Phase Adjust

Voltages present at the Slice Level (SLICELVL), Loss-of-Signal Level (LOSLVL) and Phase Adjust (PHASEADJ) pins can be used to adjust the data slicing level, the loss-of-signal alarm level, and the sampling phase position, respectively. Because these inputs are high impedance, simple turn-based potentiometers are used to apply the control voltage. The Si5100-EVB provides 50 kΩ potentiometers for each of these inputs: potentiometer R16 sets the voltage applied to the SLICELVL pin; R14 sets the voltage applied to the LOSLVL pin, and R15 sets the voltage applied to the PHASEADJ pin. The Si5110-EVB also provides 50 kΩ potentiometers for each of these inputs. Potentiometer R5 sets the voltage applied to the SLICELVL pin; R3 sets the voltage applied to the LOSLVL pin, and R4 sets the voltage applied to the PHASEADJ pin. The potentiometers are connected so the voltage applied varies from GND to VREF. Refer to the device data sheet for details on the operation of these inputs.

## Basic Test Setup

The configurations listed in Tables 1 and 3 allow easy setup of the transceiver evaluation system for operation in the line loopback, full duplex, or diagnostic loopback modes. Other configurations are supported; however, operation should first be verified in one of these modes in order to minimize the number of unknown variables.

### Line Loopback

When configured in line-loopback mode, the device passes the received/recovered data and timing to the transmitter. The transmitter buffers the data through the FIFO and filters the jitter using the loop-bandwidth selected by BWSEL[1:0]. Operation in line loopback mode is depicted in Figure 5. Jumper settings for line loopback mode are given in Tables 1, 3 (Si5100), and 4 (Si5110). This mode of operation is attainable with both versions of the motherboard.

### Full-Duplex

This mode is identical to normal operation of the device in a system. TX and RX can be asynchronous (up to ±300 ppm) so all timing is independent. TXCLK16IN is chosen as the transmitter CMU reference clock via the REFSEL pin. Operation in full-duplex mode is depicted in Figure 6. Jumper settings for full-duplex mode are given in Tables 1, 3 (Si5100), and 4 (Si5110). If the loopback motherboard is used, the full-duplex mode effectively becomes an external loopback mode, and RXCLK1 should be connected to TXCLK16IN/ TXCLK4IN to clock in the data.

### Diagnostic Loopback (Parallel Side Loopback)

This mode passes the data present on the transmit parallel inputs (TXDIN[15:0] for Si5100; TXDIN[3:0] for Si5110) to the receive parallel data outputs (RXDOUT[15:0] for Si5100; RXDOUT[3:0] for Si5110). TXCLK16IN/TXCLK4IN is chosen as the transmitter CMU reference clock via the REFSEL pin. Operation in diagnostic loopback mode is depicted in Figure 7. Jumper settings for diagnostic loopback mode are given in Tables 2, 3 (Si5100), and 4 (Si5110). The full-duplex motherboard is required for this mode.

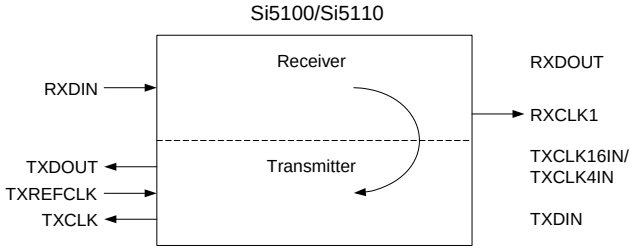



**Figure 5. Line Loopback**

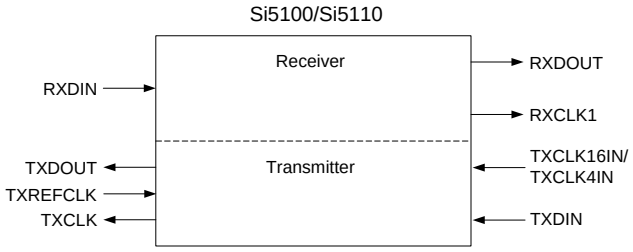



**Figure 6. Full Duplex**

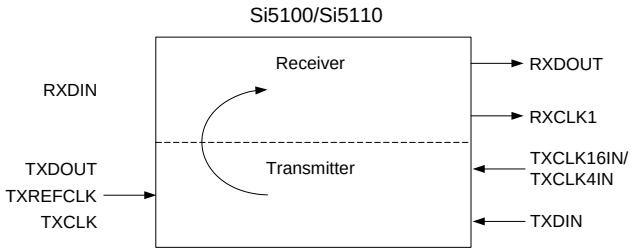



**Figure 7. Diagnostic Loopback**

Both the motherboard and daughter card are placed in line loopback mode before shipment to customers.

**Table 1. Loopback Motherboard Setup**

| Header—Pin | Signal Name | Line Loopback | Asynchronous TX/RX |
|---|---|---|---|
| JP10—2 | Voltage Select | 3.3 V | 3.3 V |
| JP1—14 | RXCLK1DSBL_N | high | high |
| JP1—11 | LTR_N | high | high |
| JP1—8 | RXSQLCH_N | low | high |
| JP1—5 | RXCLK2DIV_N | don't care | don't care |
| JP1—2 | RXCLK2DSBL_N | don't care | don't care |
| JP2—5 | TXREFRATE | high | high |
| JP2—2 | TXRESET_N | high | high |
| JP3—8 | DLBK_N | high | high |
| JP3—5 | LLBK_N | low (enables line loopback) | high |
| JP3—2 | LPTM_N | high | high |
| JP7—5 | RXREFRATE | open | open |
| JP7—2 | RXRESET_N | high | high |
| JP6—4 | FIFORST_N | tie to FIFOERR | tie to FIFOERR |

**Table 2. Full-Duplex Motherboard Setup**

| Header—Pin | Signal Name | Line Loopback | Asynchronous TX/RX | Diagnostic Loopback |
|---|---|---|---|---|
| JP8—2 | Voltage Select | 3.3 V | 3.3 V | 3.3 V |
| JP1—14 | RXCLK1DSBL_N | high | high | high |
| JP1—11 | LTR_N | high | high | high |
| JP1—8 | RXSQLCH_N | low | high | high |
| JP1—5 | RXCLK2DIV_N | don't care | don't care | don't care |
| JP1—2 | RXCLK2DSBL_N | don't care | don't care | don't care |
| JP2—5 | REFRATE | high | high | high |
| JP2—2 | RESET_N | high | high | high |
| JP3—8 | DLBK_N | high | high | low |
| JP3—5 | LLBK_N | low (enables line loopback) | high | high |
| JP3—2 | LPTM_N | high | high | high |
| JP7—5 | Si5530 REFRATE | open | open | open |
| JP7—2 | Si5530 RESET_N | high | high | high |
| JP6—4 | FIFORST_N | tie to FIFOERR | tie to FIFOERR | tie to FIFOERR |

**Table 3. Si5100 Daughter Card Setup**

| Header—Pin | Signal Name | Line Loopback | Asynchronous TX/RX | Diagnostic Loopback |
|---|---|---|---|---|
| JP1—20<br>JP1—23 | BWSEL0<br>BWSEL1 | 11<br>(for widest CMU loop bandwidth) | 11<br>(for widest CMU loop bandwidth) | 11<br>(for widest CMU loop bandwidth) |
| JP1—17 | REFSEL | high | high | high |
| JP1—14 | MODE16 | high | high | high |
| JP1—11 | TXCLKDSBL | low | low | low |
| JP1—8 | TXMSBSEL | low | low | low |
| JP1—5 | TXSQLCH_N | high | high | high |
| JP1—2 | RXMSBSEL | low | low | low |
| **Note:** Jump the VDD_IO selection jumper toward the 3.3 V side. | | | | |

**Table 4. Si5110 Daughter Card Setup**

| Header—Pin | Signal Name | Line Loopback | Asynchronous TX/RX | Diagnostic Loopback |
|---|---|---|---|---|
| JP1—20<br>JP1—23 | BWSEL0<br>BWSEL1 | 11<br>(for widest CMU loop bandwidth) | 11<br>(for widest CMU loop bandwidth) | 11<br>(for widest CMU loop bandwidth) |
| JP1—17 | REFSEL | high | high | high |
| JP1—14 | TXCLKDSBL | low | low | low |
| JP1—11 | TXMSBSEL | low | low | low |
| JP1—8 | TXSQLCH_N | high | high | high |
| JP1—5 | SLICEMODE | low | low | low |
| JP1—2 | RXMSBSEL | low | low | low |
| **Note:** Jump the VDD_IO selection jumper toward the 3.3 V side. | | | | |

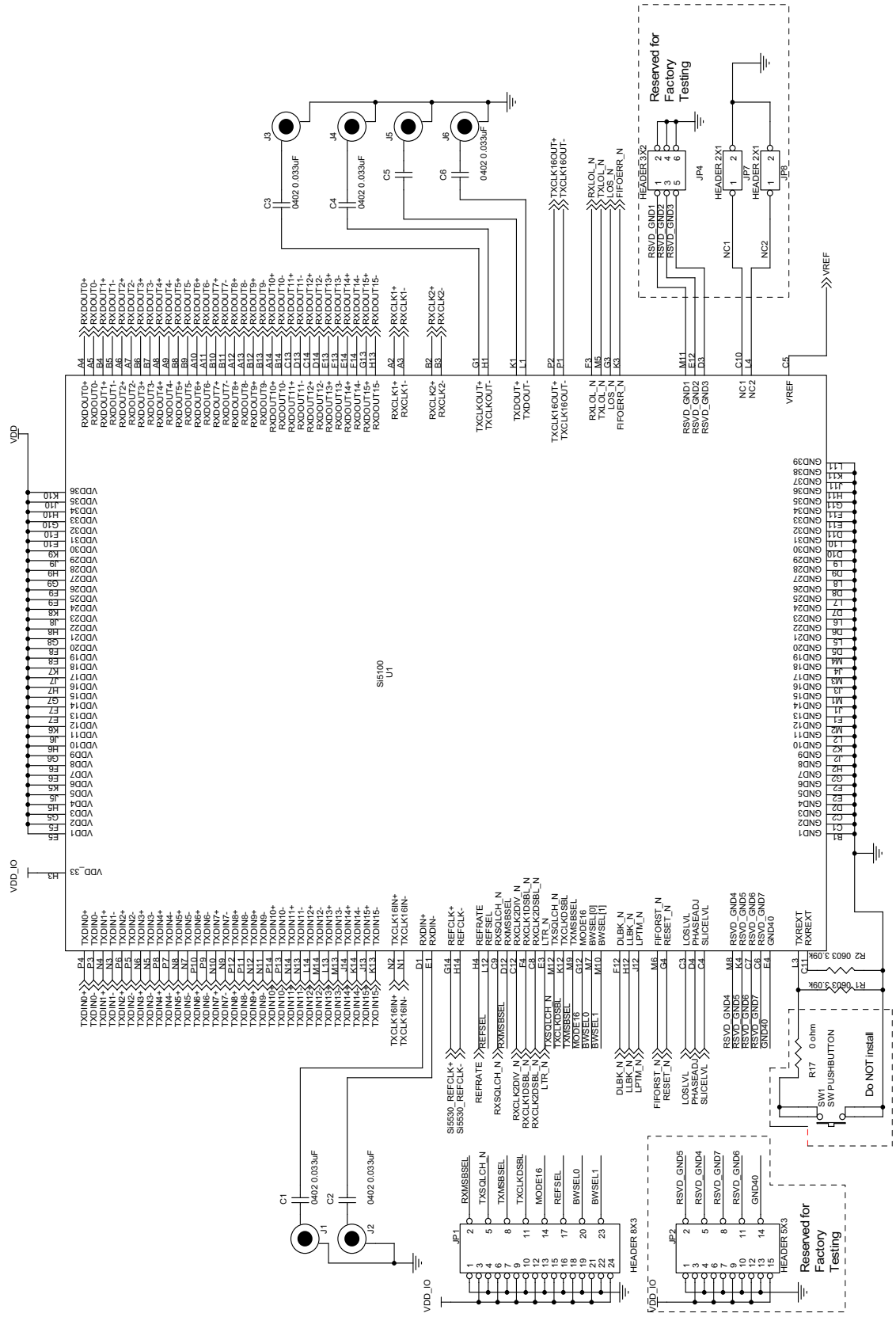



**Figure 8. Si5100-EVB Daughter Card Schematic (page 1 of 3)**

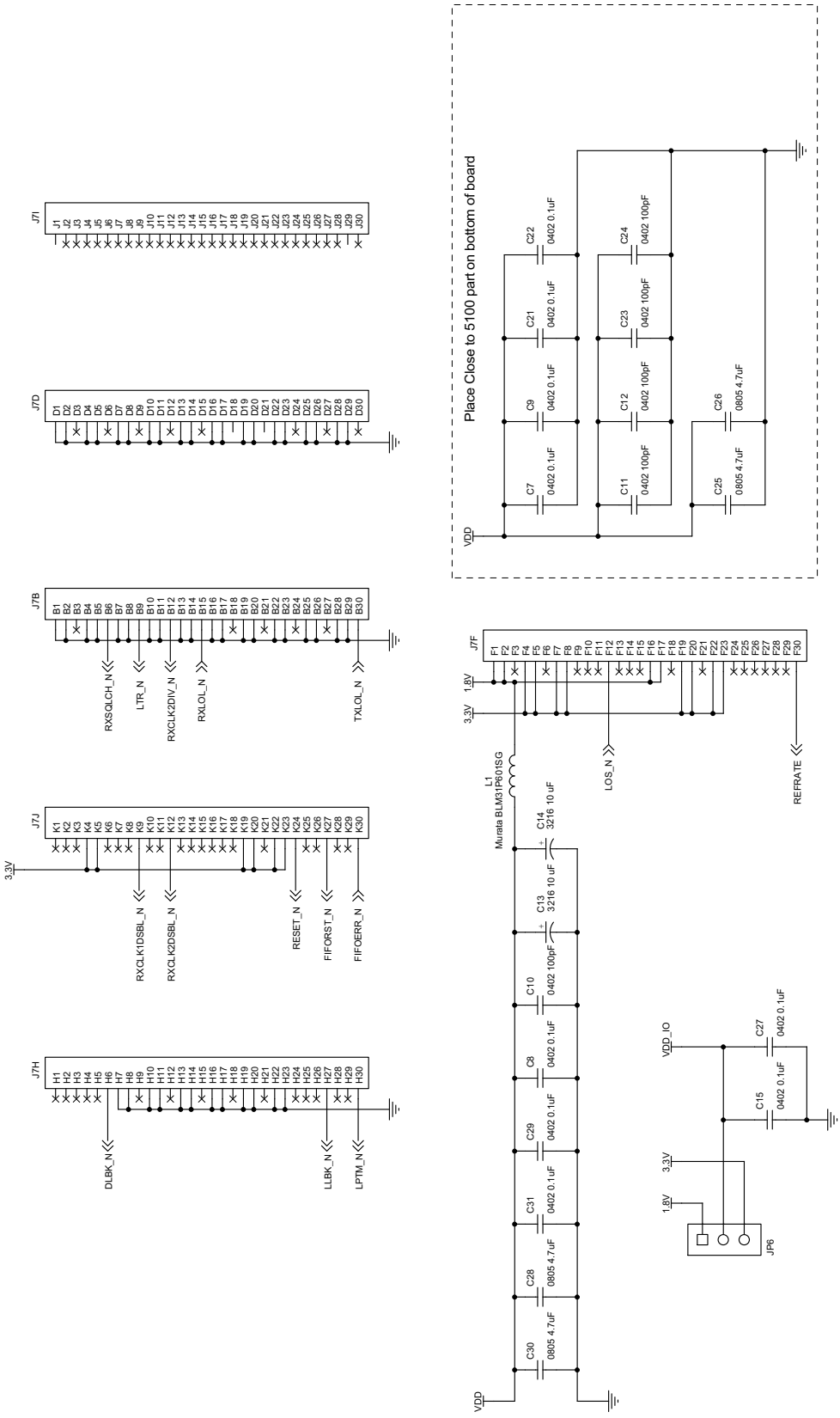



**Figure 9. Si5100-EVB Daughter Card Schematic (page 2 of 3)**

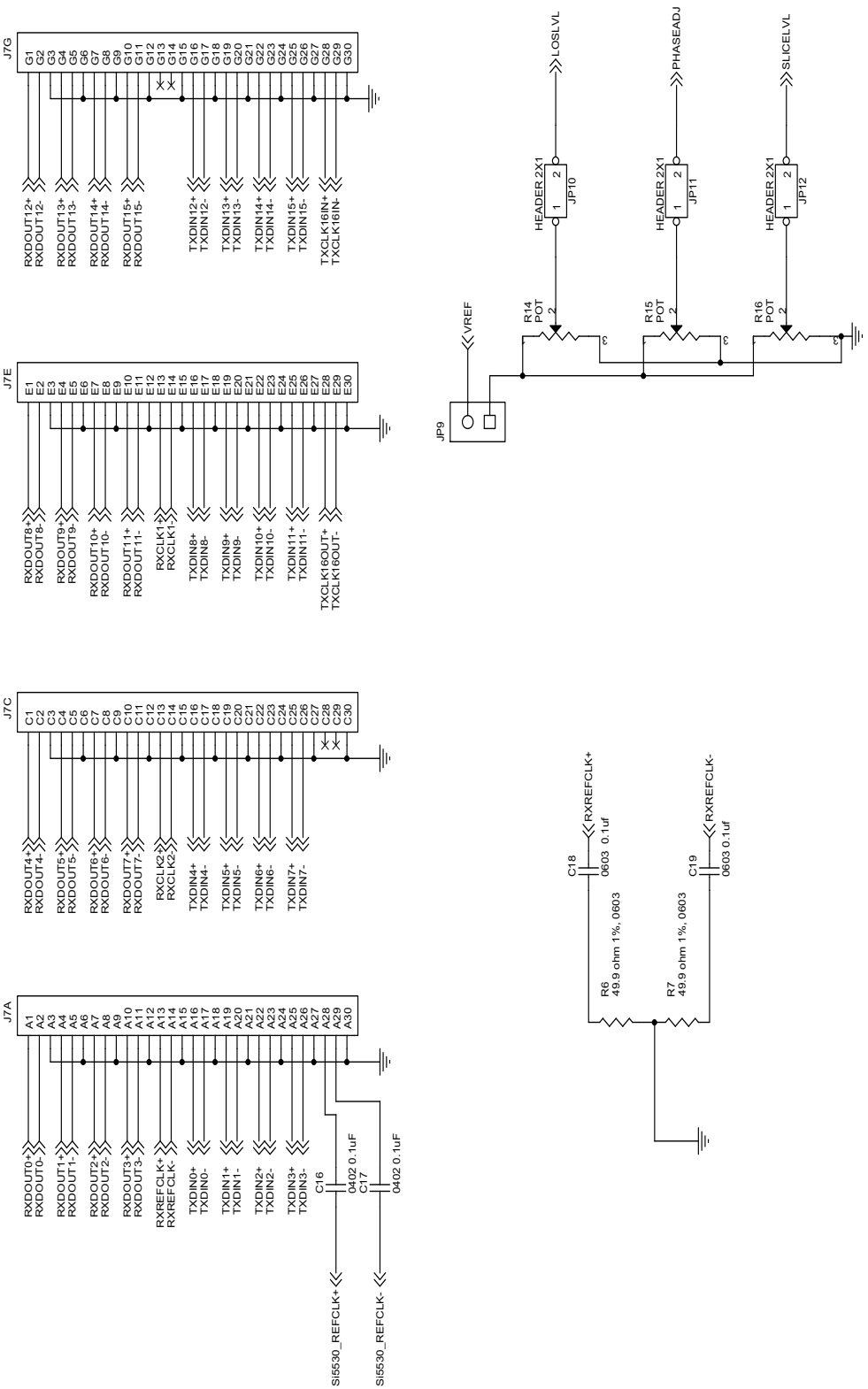



**Figure 10. Si5100-EVB Daughter Card Schematic (page 3 of 3)**

## Bill of Materials: Si5100-EVB Daughter Card Assembly Revision D-01

| Si5100EVB Assy Rev D-01 BOM | | | |
|---|---|---|---|
| | | | |
| **Reference** | **Description** | **Manu Number** | **Manufacturer** |
| C1,C2,C3,C4,C5,C6 | CAP, SM, 0.033 uF, 0402 | C0402X7R160333KNE | VENKEL |
| C7,C8,C9,C15,C16,C17, | CAP, SM, 0.1 uF, 0402 | C0402X7R160104KNE | VENKEL |
| C21,C22,C27,C29,C31 | | | |
| C10,C11,C12,C23,C24 | CAP, SM, 100 pF, 0402 | C0402C0G500-101JNE | VENKEL |
| C14,C13 | CAP, SM, 10 uF, TANTALUM, 3216 | TA010TCM106KAR | VENKEL |
| C18,C19 | CAP, SM, 0.1 uF, 0603 | C0603X7R160-104KNE | VENKEL |
| C25,C26,C28,C30 | CAP,SM,4.7UF,6.3V,X7R,0805 | CEJMK212BJ475KG-T | TAIYO YUDEN |
| JP1 | CONNECTOR, HEADER, 8X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP2 | CONNECTOR, HEADER, 5X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP4 | CONNECTOR, HEADER, 3X2 | 2380-6121TN or 2340-6111TN | 3M |
| JP6 | CONNECTOR, HEADER, 3X1 | 2380-6121TN or 2340-6111TN | 3M |
| JP7,JP8,JP9,JP10,JP11, | CONNECTOR, HEADER, 2X1 | 2380-6121TN or 2340-6111TN | 3M |
| JP12 | | | |
| J1,J2,J3,J4,J5,J6 | CONNECTOR, SMA, NOTCH MOUNT | 82 SMA-S50-1-45/111 NE | HUBER SUHNER |
| J7 | CONN,SM,RECPT,MEGARRAY,300 POS BGA | 84502-101 | FCI/BERG |
| L1 | FERRITE,SM,600 OHM,1500mA | BLM31P601SGPT | MURATA |
| R1,R2 | RESISTOR, SM, 3.09K, 1%, 0603 | CR0603-16W-3091FT | VENKEL |
| R6,R7 | RES,SM,49.9,1%,0603 | CR0603-16W-49R9FT | VENKEL |
| R14,R15,R16 | POT,50K,10%,MULTITURN TRIMMER | T93YA-50K-10%-D06 | VISHAY/DALE |
| U1 | Si5100 Rev D Device | Si5100 Rev D | SILICON LABORATORIES |
| PCB | Printed Circuit Board | Si5100-EVB Daughter Card PCB Rev D | SILICON LABORATORIES |
| | | | |
| **No Load** | | | |
| SW1 | SWITCH, PUSH BUTTON, MINIATURE | 101-0161 | MOUSER |
| R17 | RES,SM,0,0603 | CR0603-16W-000T | VENKEL |

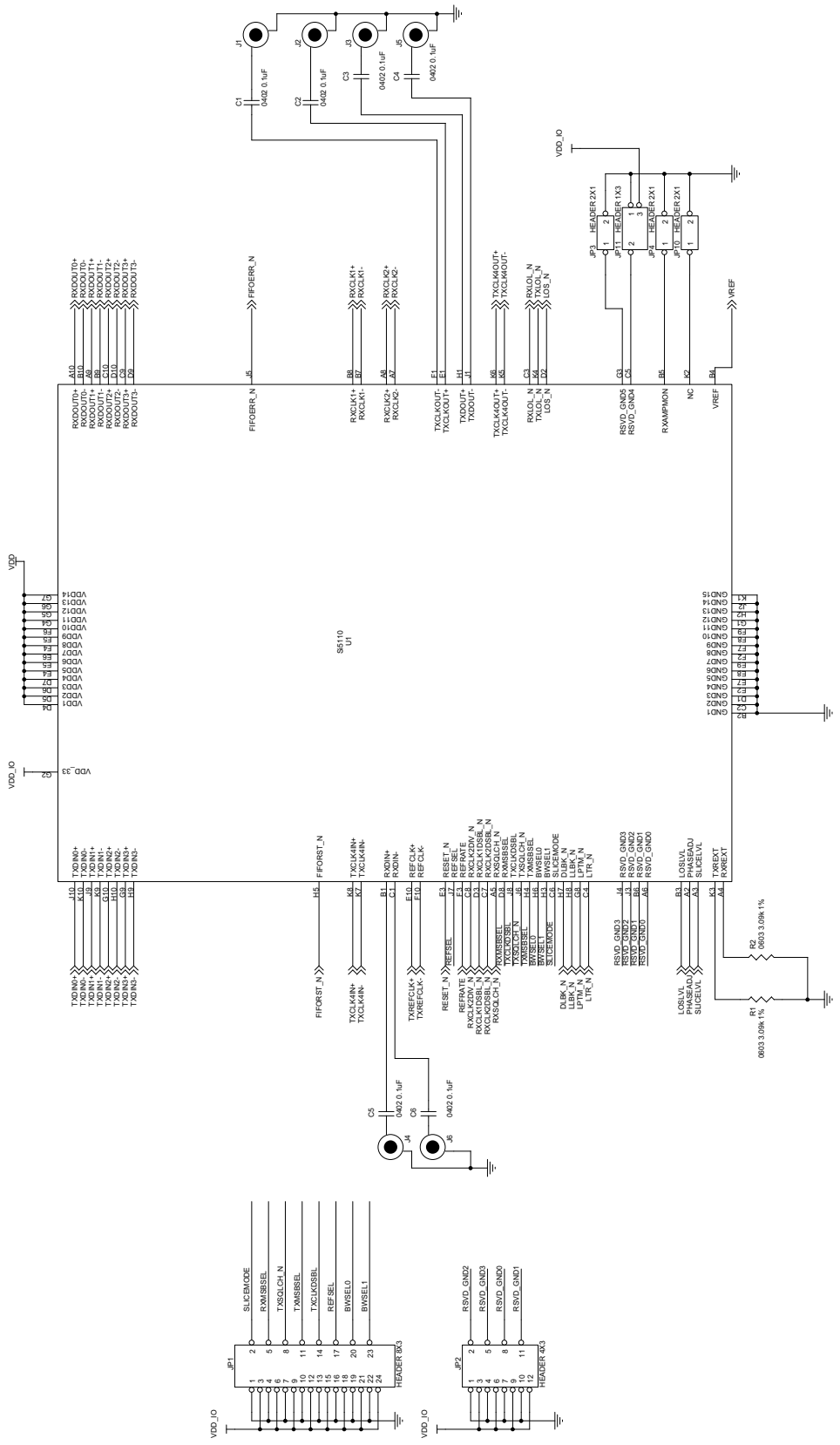



**Figure 11. Si5110-EVB Daughter Card Schematic (page 1 of 3)**

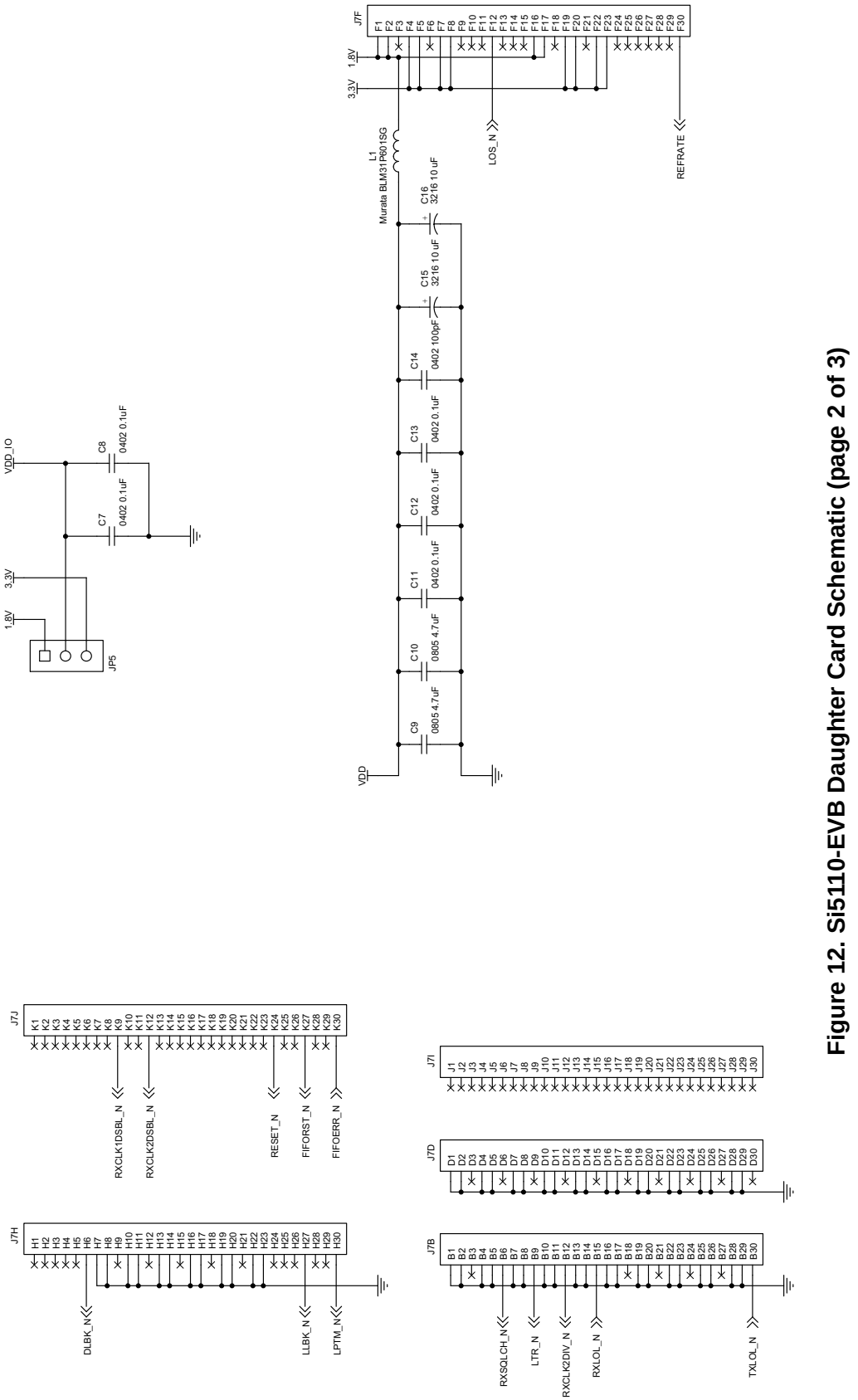



**Figure 12. Si5110-EVB Daughter Card Schematic (page 2 of 3)**

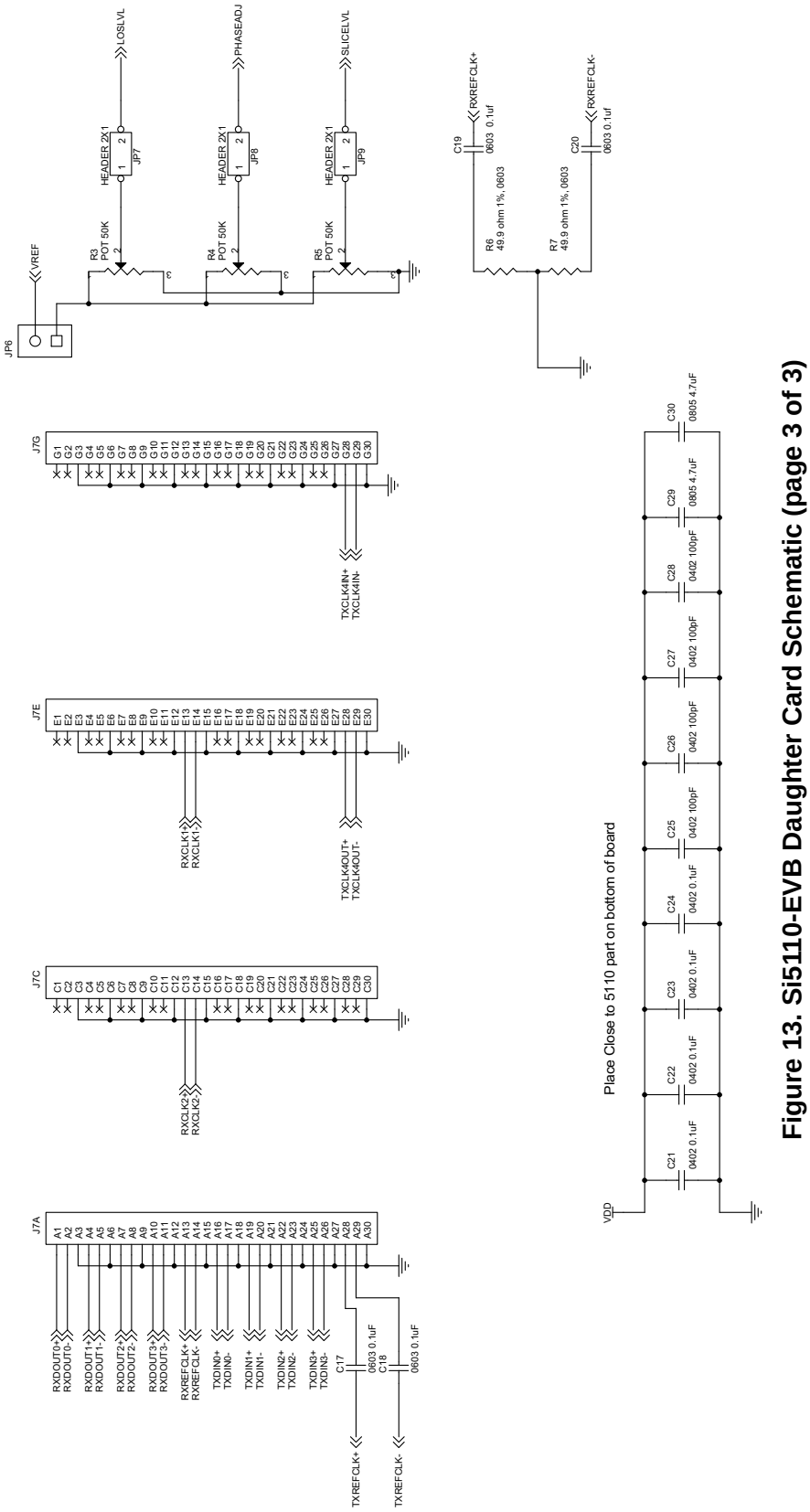



**Figure 13. Si5110-EVB Daughter Card Schematic (page 3 of 3)**

## Bill of Materials: Si5110-EVB Daughter Card Assembly Revision D-01

| Si5110 EVB Daughter Card Assy Rev. E-01 BOM | | | |
|---|---|---|---|
| | | | |
| **Reference** | **Part Desc** | **Part Number** | **Manufacturer** |
| | | | |
| C1,C2,C3,C4,C5,C6,C7,C8 | CAP,SM,0.1UF,16V,10%,X7R,0402 | C0402X7R160-104KNE | VENKEL |
| C11,C12,C13,C21,C22,C23 | | | |
| C24 | | | |
| C9,C10,C29,C30 | CAP,SM,4.7UF,6.3V,X7R,0805 | CEJMK212BJ475KG-T | TAIYO YUDEN |
| C14,C25,C26,C27,C28 | CAP,SM,100PF,50V,5%,C0G,0402 | C0402C0G500-101JNE | VENKEL |
| C15,C16 | CAP,SM,10UF,10V,10%,TANTALUM,3216 | TA010TCM106KAR | VENKEL |
| C17,C18,C19,C20 | CAP,SM,0.1UF,16V,20%,X7R,0603 | C0603X7R160-104KNE | VENKEL |
| JP1 | CONN,HEADER,8X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP5 | CONN,HEADER,3X1 | 2380-6121TN or 2340-6111TN | 3M |
| JP4,JP6,JP7,JP8,JP9 | CONN,HEADER,2X1 | 2380-6121TN or 2340-6111TN | 3M |
| J1,J2,J3,J4,J5,J6 | CONNECTOR, SMA, NOTCH MOUNT | 82 SMA-S50-1-45/111 NE | HUBER SUHNER |
| J7 | CONN,SM,RECPT,MEGARRAY,300 POS BGA | 84502-101 | FCI/BERG |
| L1 | FERRITE,SM,600 OHM,1500mA | BLM31P601SGPT | MURATA |
| R2,R1 | RES,SM,3.09K,1%,0603 | CR0603-16W-3091FT | VENKEL |
| R3,R4,R5 | POT,50K,10%,MULTITURN TRIMMER | T93YA-50K-10%-D06 | VISHAY/DALE |
| R6,R7 | RES,SM,49.9,1%,0603 | CR0603-16W-49R9FT | VENKEL |
| U1 | Si5110 Rev E Device | Si5110-BC | SILICON LABS |
| PCB | Printed Circuit Board | Si5110-EVB Daughter Card PCB Rev C | SILICON LABS |
| | | | |
| | | | |
| JP2 | CONN,HEADER,4X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP3, JP10 | CONN,HEADER,2X1 | 2380-6121TN or 2340-6111TN | 3M |
| JP11 | CONN,HEADER,1X3 | 2380-6121TN or 2340-6111TN | 3M |

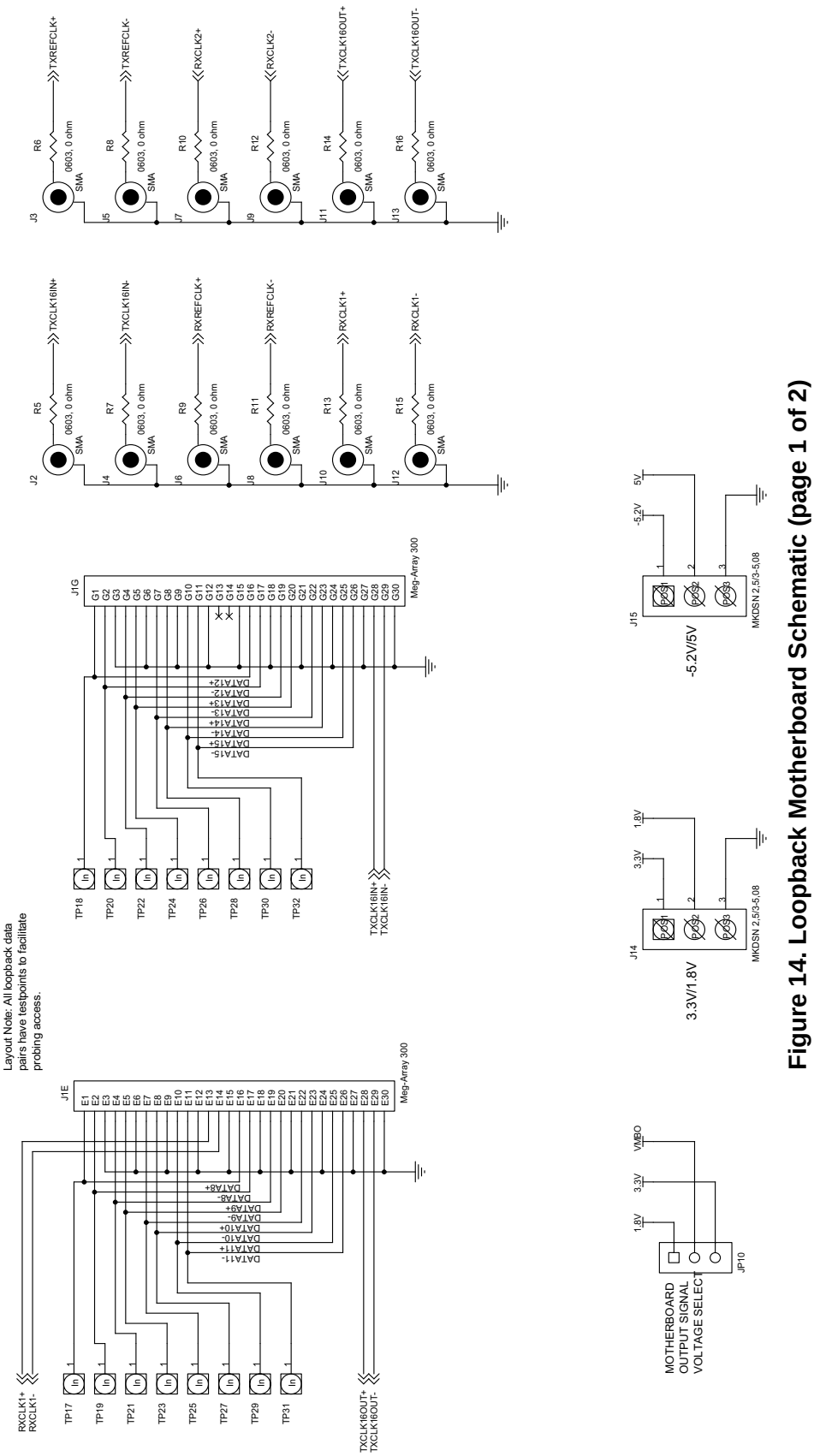



**Figure 14. Loopback Motherboard Schematic (page 1 of 2)**

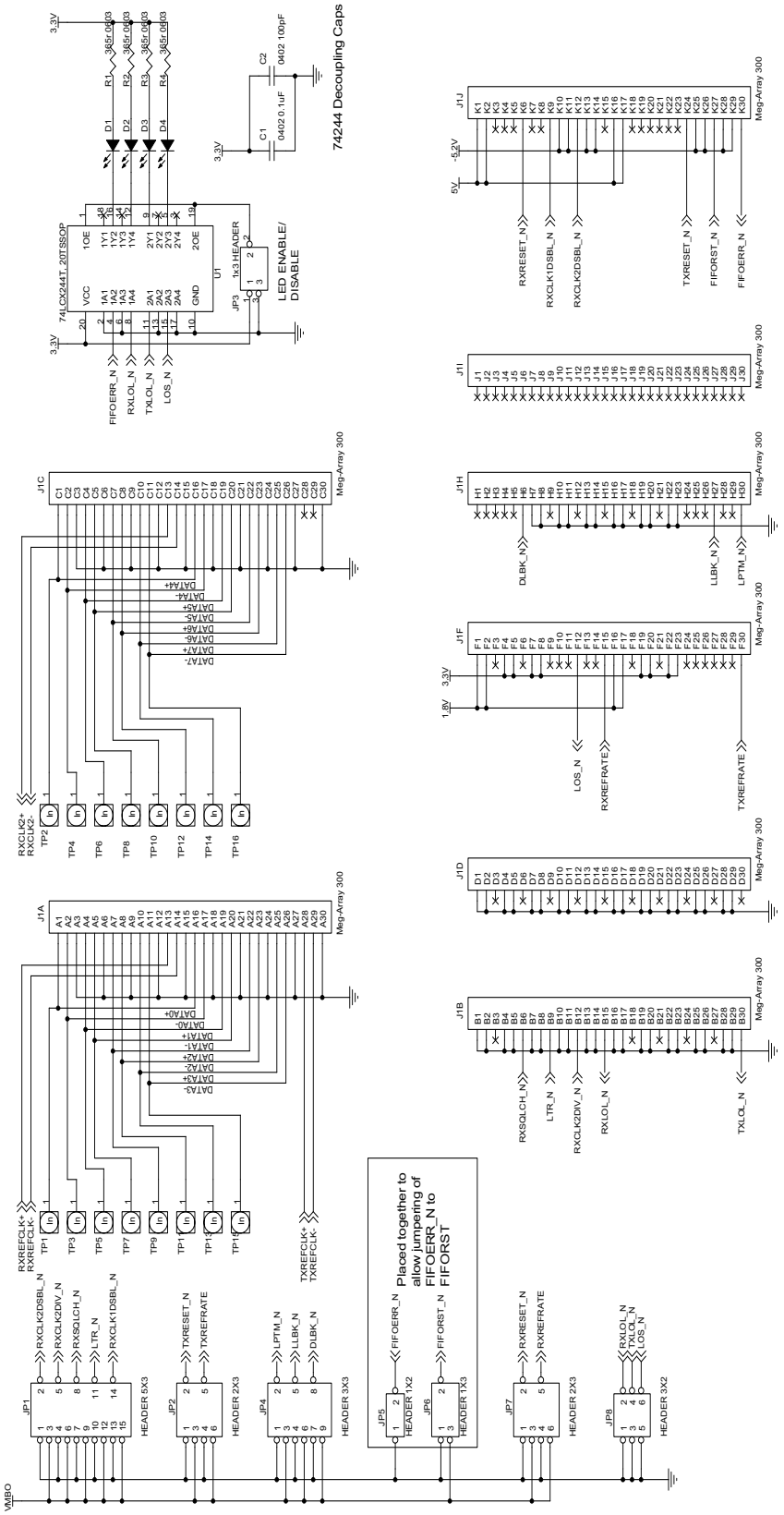



**Figure 15. Loopback Motherboard Schematic (page 2 of 2)**

## Bill of Materials: Loopback Motherboard Assembly Revision A-01

| Si5100 Loopback Motherboard Assy Rev A-01 | | | |
|---|---|---|---|
| | | | |
| **Reference** | **Part Desc** | **Part Number** | **Manufacturer** |
| | | | |
| | | | |
| C1 | CAP,SM,0.1UF,16V,10%,X7R,0402 | C0402X7R160-104KNE | VENKEL |
| C2 | CAP,SM,100PF,50V,5%,C0G,0402 | C0402C0G500-101JNE | VENKEL |
| D1,D2,D3,D4 | LED,SM,RED | LN1271RAL-TR | PANASONIC |
| JP1 | CONN,HEADER,5X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP2,JP7 | CONN,HEADER,2X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP3,JP6 | CONN,HEADER,1X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP4 | CONN,HEADER,3X3 | 2380-6121TN or 2340-6111TN | 3M |
| JP5 | CONN,HEADER,1X2 | 2380-6121TN or 2340-6111TN | 3M |
| JP8 | CONN,HEADER,3X2 | 2380-6121TN or 2340-6111TN | 3M |
| JP10 | CONN,HEADER,3X1 | 2380-6121TN or 2340-6111TN | 3M |
| J1 | CONNECTOR,SM,300 POS,BGA | 84500-02 | BERG |
| J2,J3,J4,J5,J6,J7,J8,J9, | CONNECTOR,SMA,SURFACE MOUNT | 142-0711-201 | JOHNSON COMPONENTS |
| J10,J11,J12,J13 | | | |
| J15,J14 | CONNECTOR,POWER,3 POSITION | 1729021 | PHOENIX CONTACT |
| R1,R2,R3,R4 | RESISTOR, SM, 365 OHM, 1%, 0603 | CR0603-16W-121JT | VENKEL |
| R5,R6,R7,R8,R9,R10,R11, | RES,SM,0,0402 | CR0402-16W-000T | VENKEL |
| R12,R13,R14,R15,R16 | | | |
| TP1,TP2,TP3,TP4,TP5,TP6, | TEST POINTS ON PCB | N/A | N/A |
| TP7,TP8,TP9,TP10,TP11, | | | |
| TP12,TP13,TP14,TP15,TP16, | | | |
| TP17,TP18,TP19,TP20,TP21, | | | |
| TP22,TP23,TP24,TP25,TP26, | | | |
| TP27,TP28,TP29,TP30,TP31, | | | |
| TP32 | | | |
| U1 | IC,SM,74LCX244,20TSSOP | 74LCX244MTC | FAIRCHILD |
| PCB | Printed Circuit Board | Si5100-EVB Loopback Motherboard PCB Rev A | SILICON LABORATORIES |

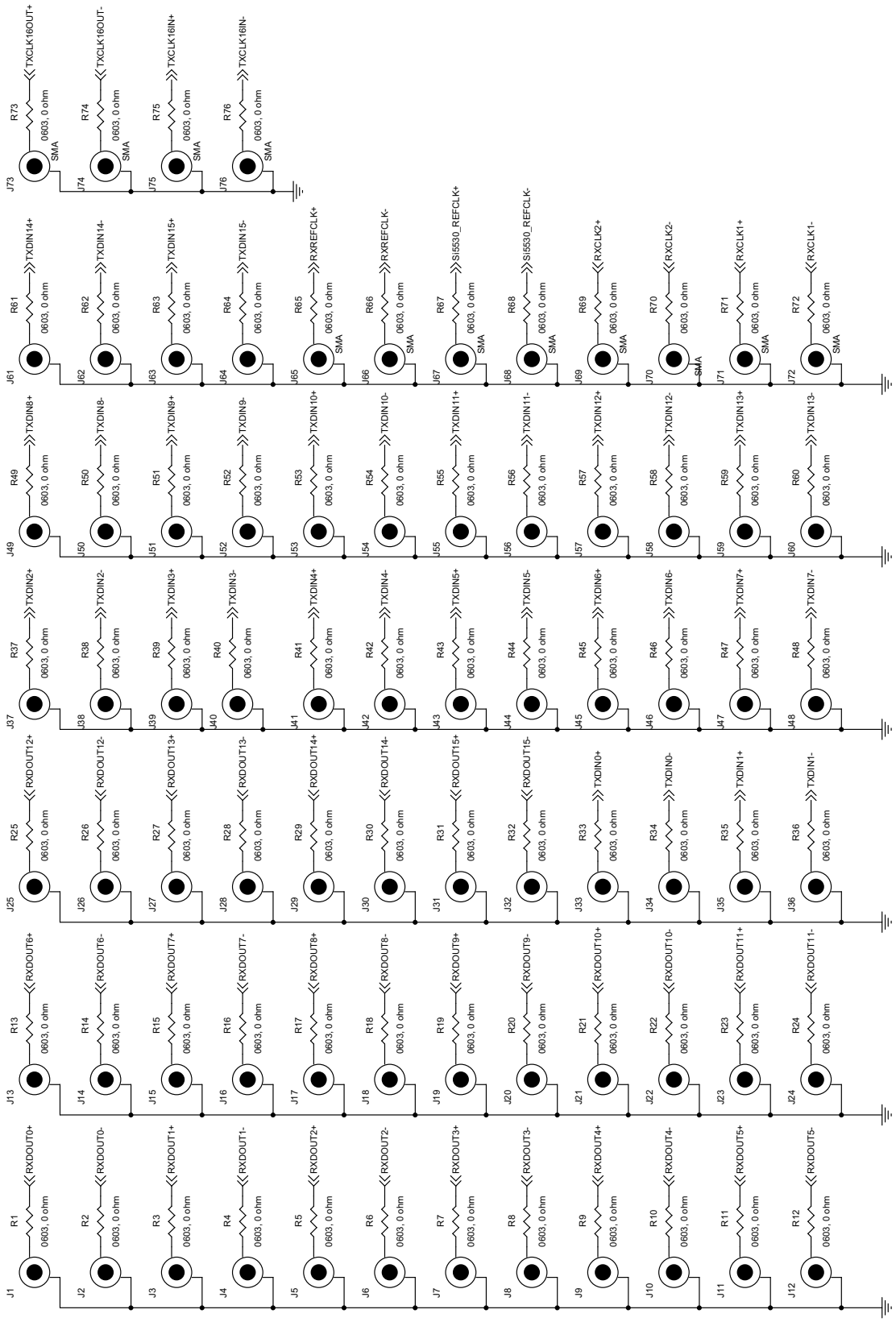



**Figure 16. Full-Duplex Motherboard Schematic (page 1 of 2)**

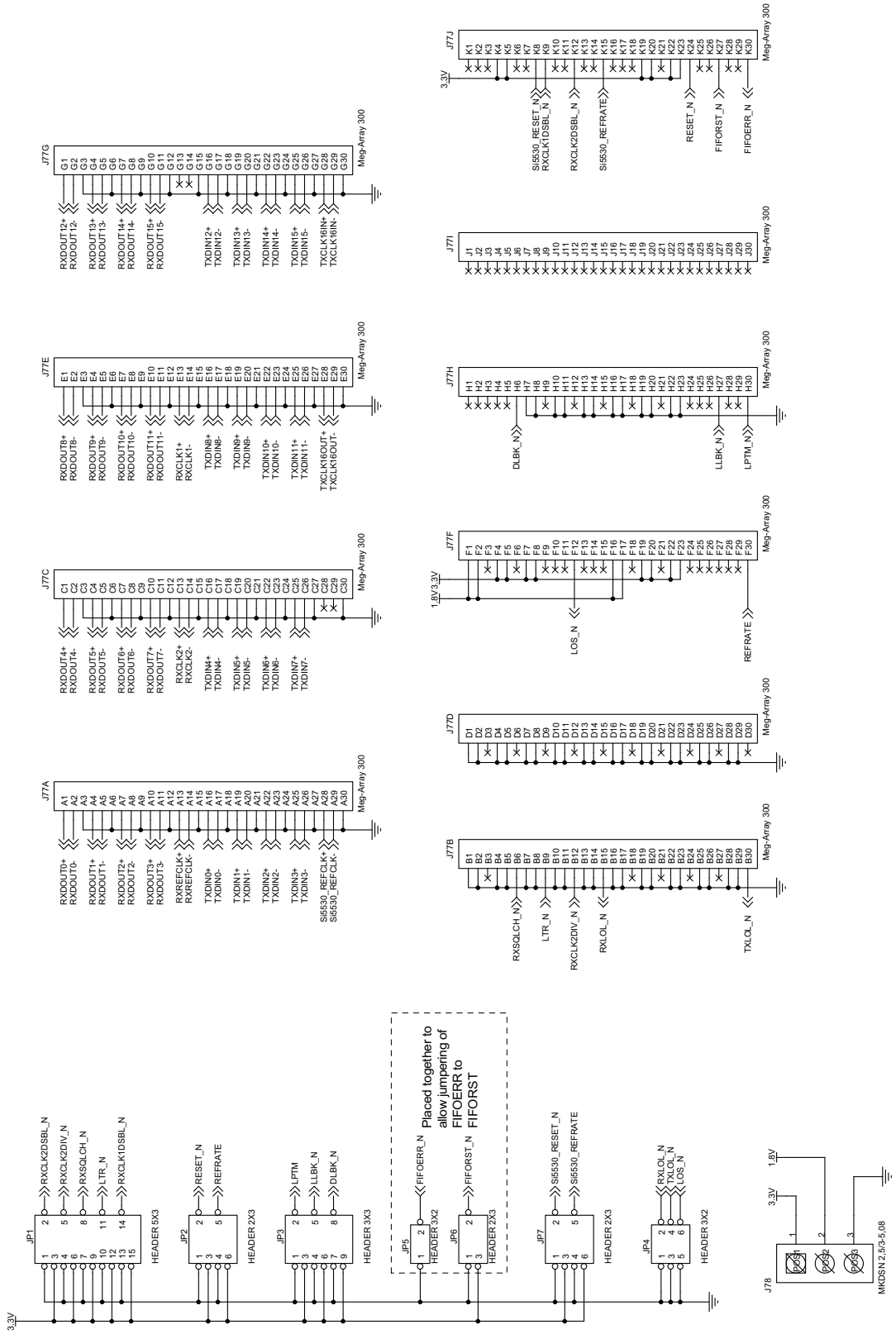



**Figure 17. Full-Duplex Motherboard Schematic (page 2 of 2)**

## Bill of Materials: Full-Duplex Motherboard Assembly Revision C-01

| Si5100 Motherboard Assy Rev C-01 BOM | | | |
|---|---|---|---|
| | | | |
| **Reference** | **Part Desc** | **Part Number** | **Manufacturer** |
| R1,R2,R3,R4,R5,R6,R7,R8, | RES,SM,0,0402 | CR0402-16W-000T | VENKEL |
| R9,R10,R11,R12,R13,R14, | | | |
| R15,R16,R17,R18,R19,R20, | | | |
| R21,R22,R23,R24,R25,R26, | | | |
| R27,R28,R29,R30,R31,R32, | | | |
| R33,R34,R35,R36,R37,R38, | | | |
| R39,R40,R41,R42,R43,R44, | | | |
| R45,R46,R47,R48,R49,R50, | | | |
| R51,R52,R53,R54,R55,R56, | | | |
| R57,R58,R59,R60,R61,R62, | | | |
| R63,R64,R65,R66,R67,R68, | | | |
| R69,R70,R71,R72,R73,R74, | | | |
| R75,R76 | | | |
| JP1 | CONNECTOR,HEADER,5X3 | 2340-6111TN or 2380-6121TN | 3M |
| JP2,JP4,JP7 | CONNECTOR,HEADER,3X2 | 2340-6111TN or 2380-6121TN | 3M |
| JP3 | CONNECTOR,HEADER,3X3 | 2340-6111TN or 2380-6121TN | 3M |
| JP5 | CONNECTOR,HEADER,2X1 | 2340-6111TN or 2380-6121TN | 3M |
| JP6 | CONNECTOR,HEADER,3X1 | 2340-6111TN or 2380-6121TN | 3M |
| J1,J2,J3,J4,J5,J6,J7,J8, | CONNECTOR,SMA,SURFACE MOUNT | 142-0711-201 | JOHNSON COMPONENTS |
| J9,J10,J11,J12,J13,J14, | | | |
| J15,J16,J17,J18,J19,J20, | | | |
| J21,J22,J23,J24,J25,J26, | | | |
| J27,J28,J29,J30,J31,J32, | | | |
| J33,J34,J35,J36,J37,J38, | | | |
| J39,J40,J41,J42,J43,J44, | | | |
| J45,J46,J47,J48,J49,J50, | | | |
| J51,J52,J53,J54,J55,J56, | | | |
| J57,J58,J59,J60,J61,J62, | | | |
| J63,J64,J65,J66,J67,J68, | | | |
| J69,J70,J71,J72,J73,J74, | | | |
| J75,J76 | | | |
| J77 | CONNECTOR,SM,300 POS,BGA | 84500-02 | BERG |
| J78 | CONNECTOR,POWER,3 POSITION | 1729021 | PHOENIX CONTACT |
| PCB | Printed Circuit Board | Si5100-EVB Motherboard PCB Rev C | SILICON LABORATORIES |

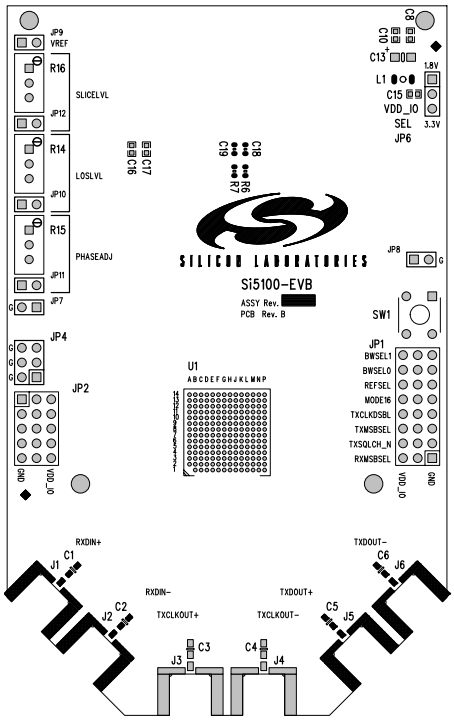



**Figure 18. Si5100-EVB Component Side Assembly (Daughter Card)**

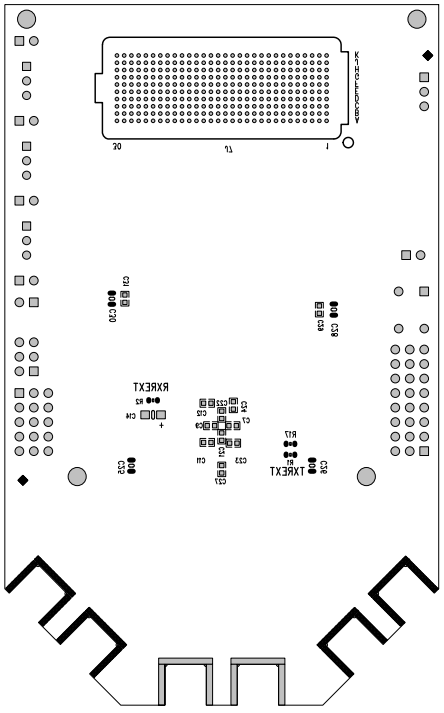


**Figure 19. Si5100-EVB Solder Side Assembly (Daughter Card)**

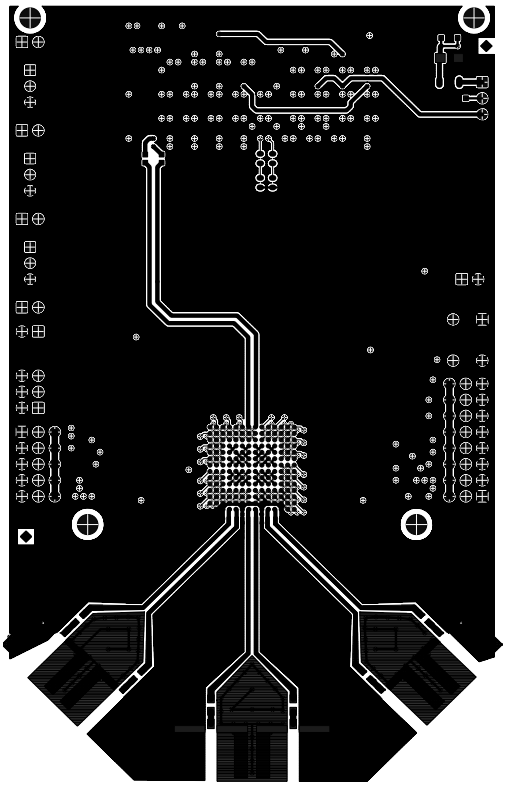


**Figure 20. Si5100-EVB Layer 1—Component Side (Daughter Card)**

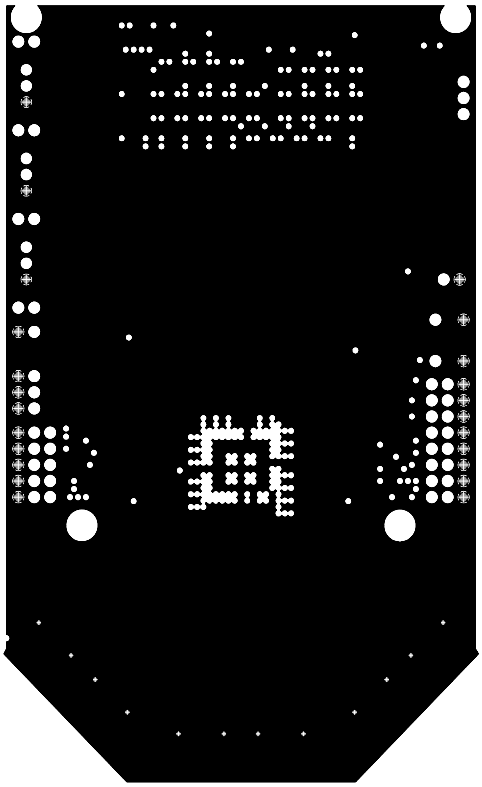


**Figure 21. Si5100-EVB Layer 2—GND1 Plane (Daughter Card)**

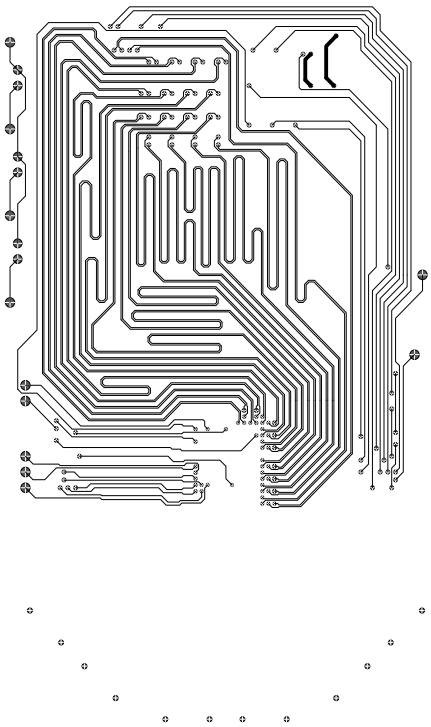


Figure 22. Si5100-EVB Layer 3—Signal Plane (Daughter Card)

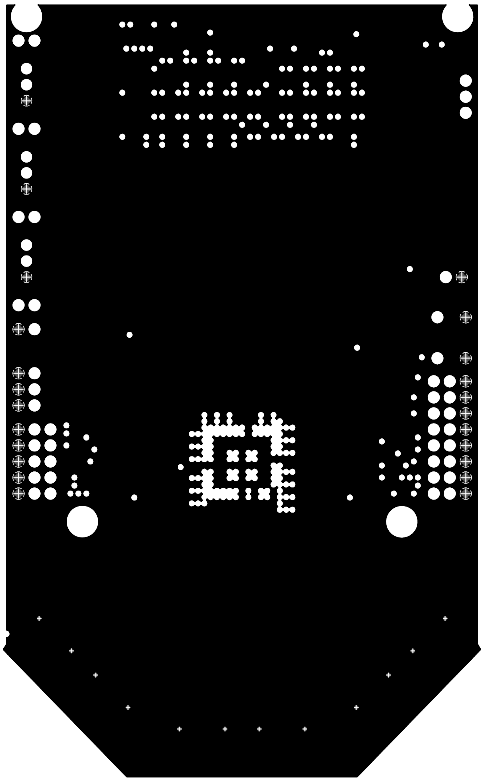


Figure 23. Si5100-EVB Layer 4—GND2 Plane (Daughter Card)

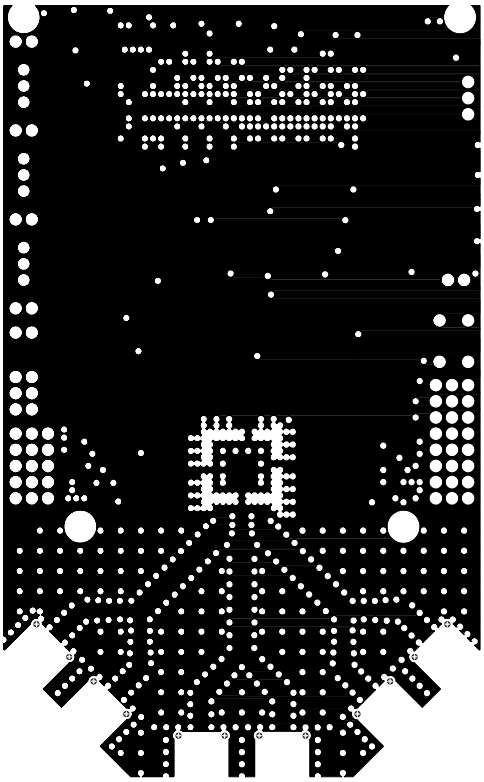


Figure 24. Si5100-EVB Layer 5—VDD Plane (Daughter Card)

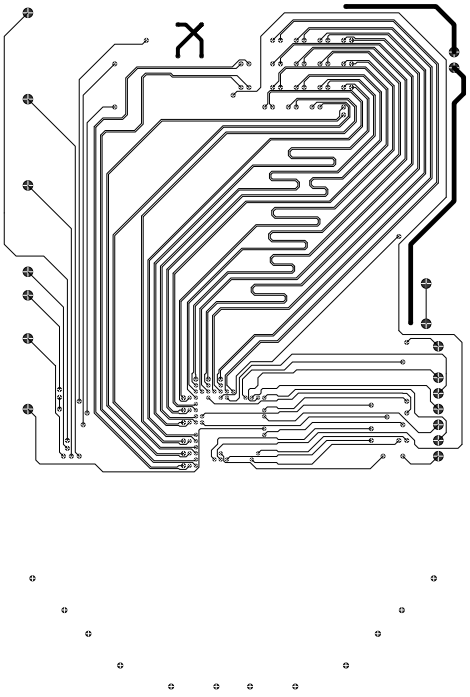


Figure 25. Si5100-EVB Layer 6—Signal Plane (Daughter Card)

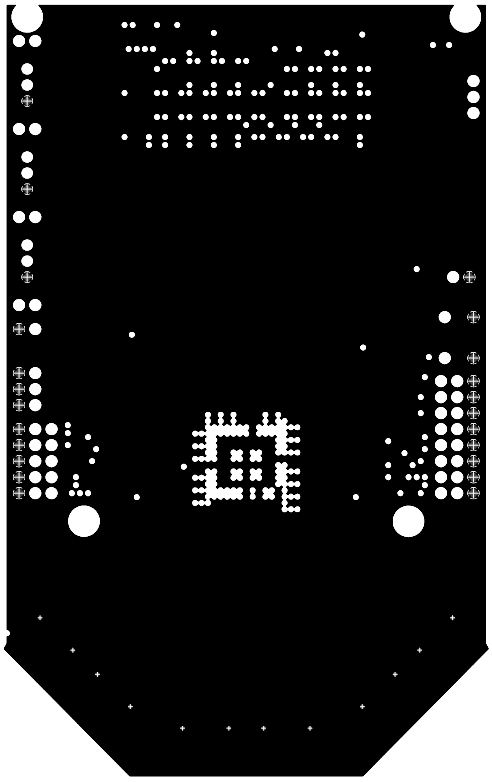


**Figure 26. Si5100-EVB Layer 7—GND3 Plane (Daughter Card)**

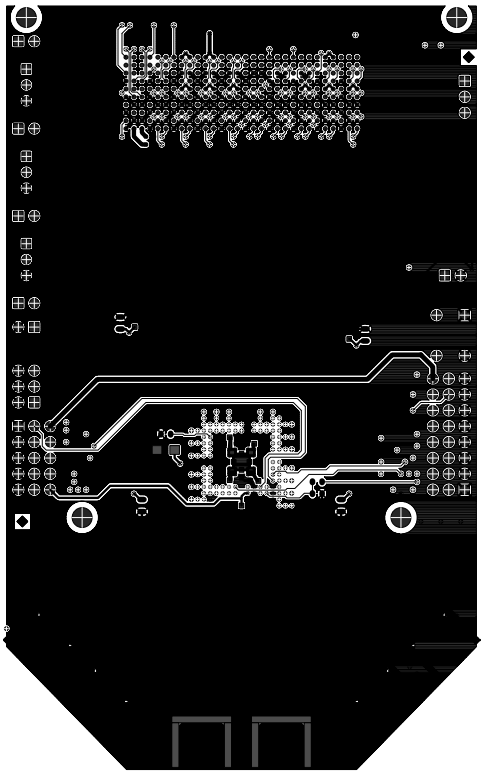


**Figure 27. Si5100-EVB Layer 8—Solder Side (Daughter Card)**

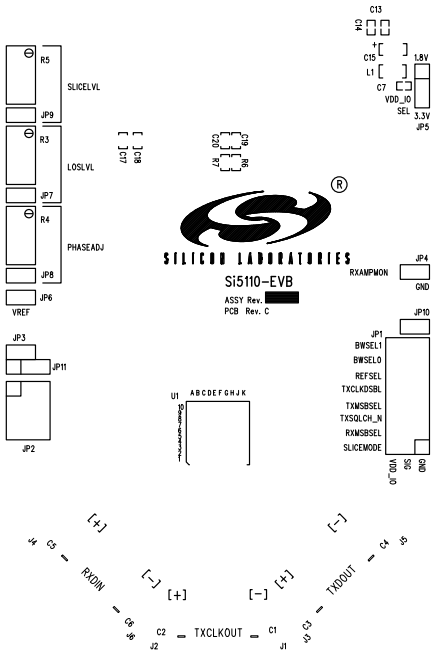



**Figure 28. Si5110-EVB Component Side Assembly (Daughter Card)**

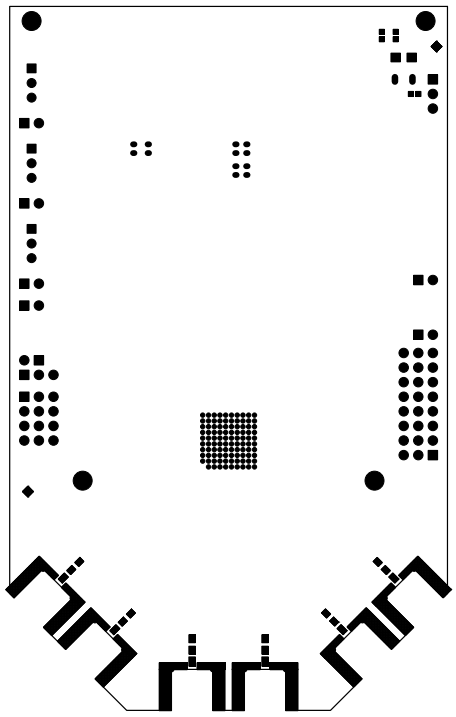


**Figure 29. Si5110-EVB Solder Side Assembly (Daughter Card)**

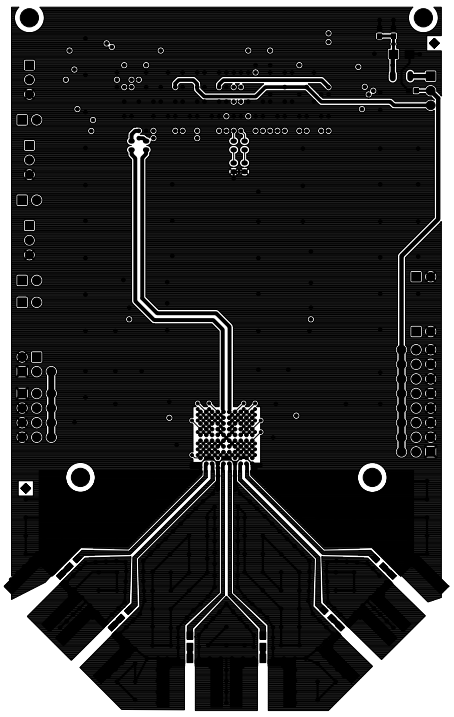


**Figure 30. Si5110-EVB Layer 1—Component Side (Daughter Card)**

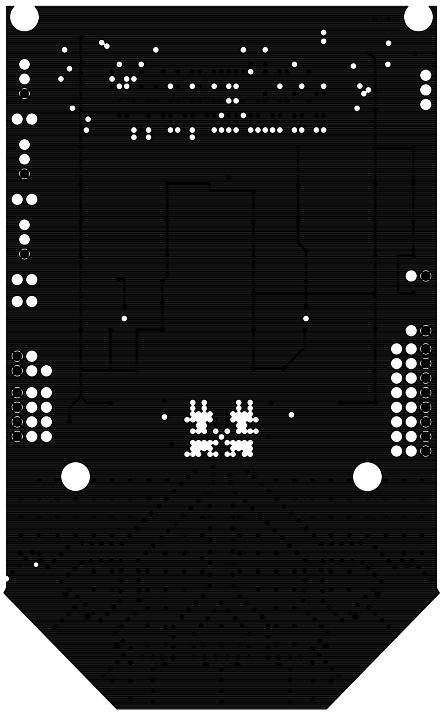


**Figure 31. Si5110-EVB Layer 2—GND1 Plane (Daughter Card)**

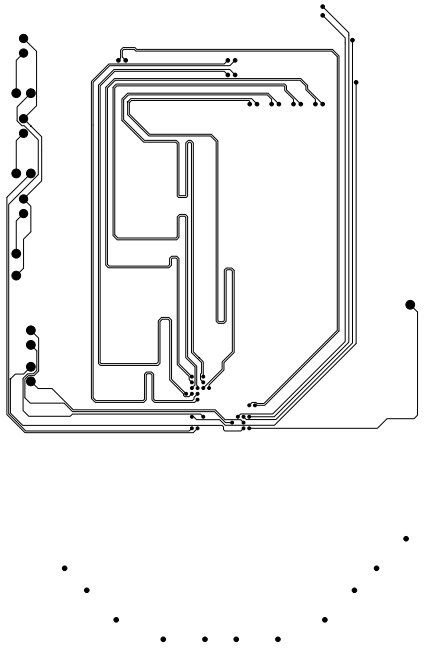


Figure 32. Si5110-EVB Layer 3—Signal Plane (Daughter Card)

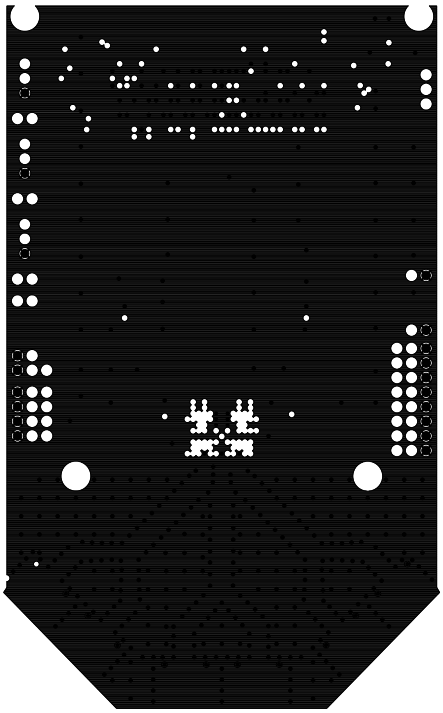


Figure 33. Si5110-EVB Layer 4—GND2 Plane (Daughter Card)

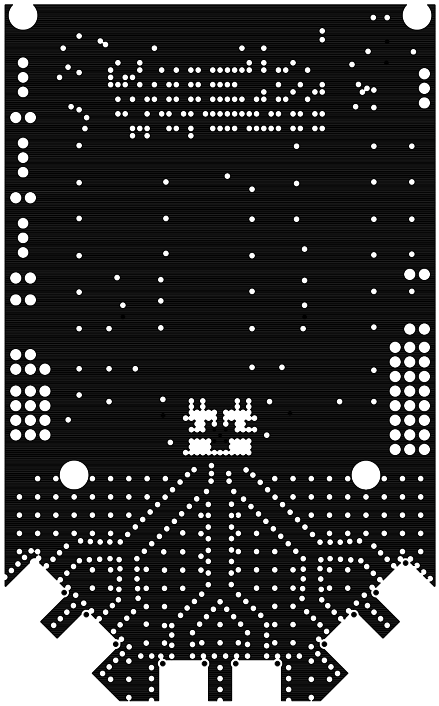


**Figure 34. Si5110-EVB Layer 5—VDD Plane (Daughter Card)**

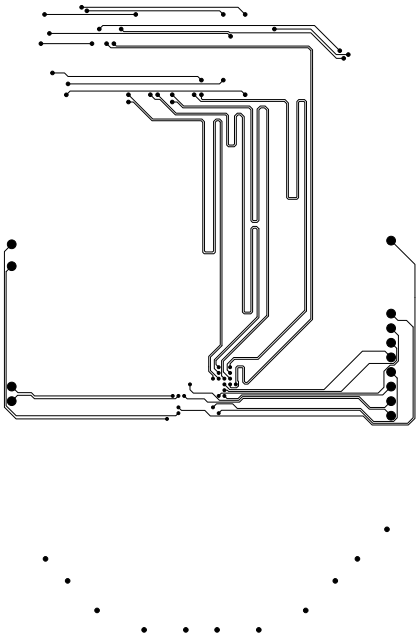


**Figure 35. Si5110-EVB Layer 6—Signal Plane (Daughter Card)**

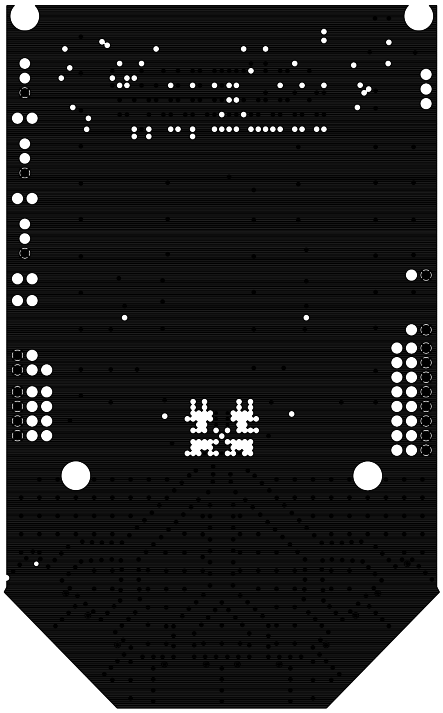


**Figure 36. Si5110-EVB Layer 7—GND3 Plane (Daughter Card)**

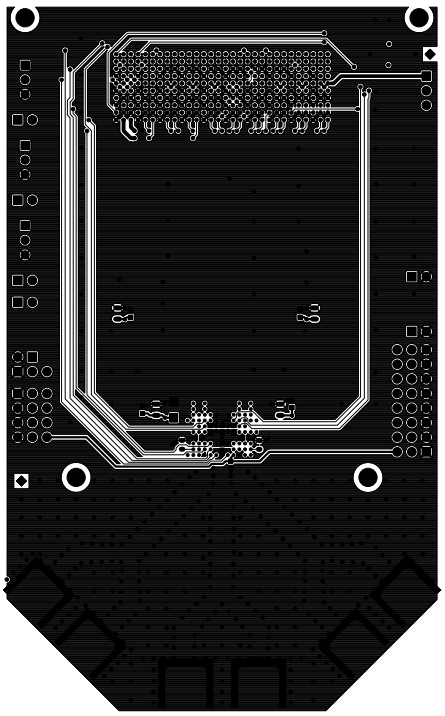


**Figure 37. Si5110-EVB Layer 8—Solder Side (Daughter Card)**

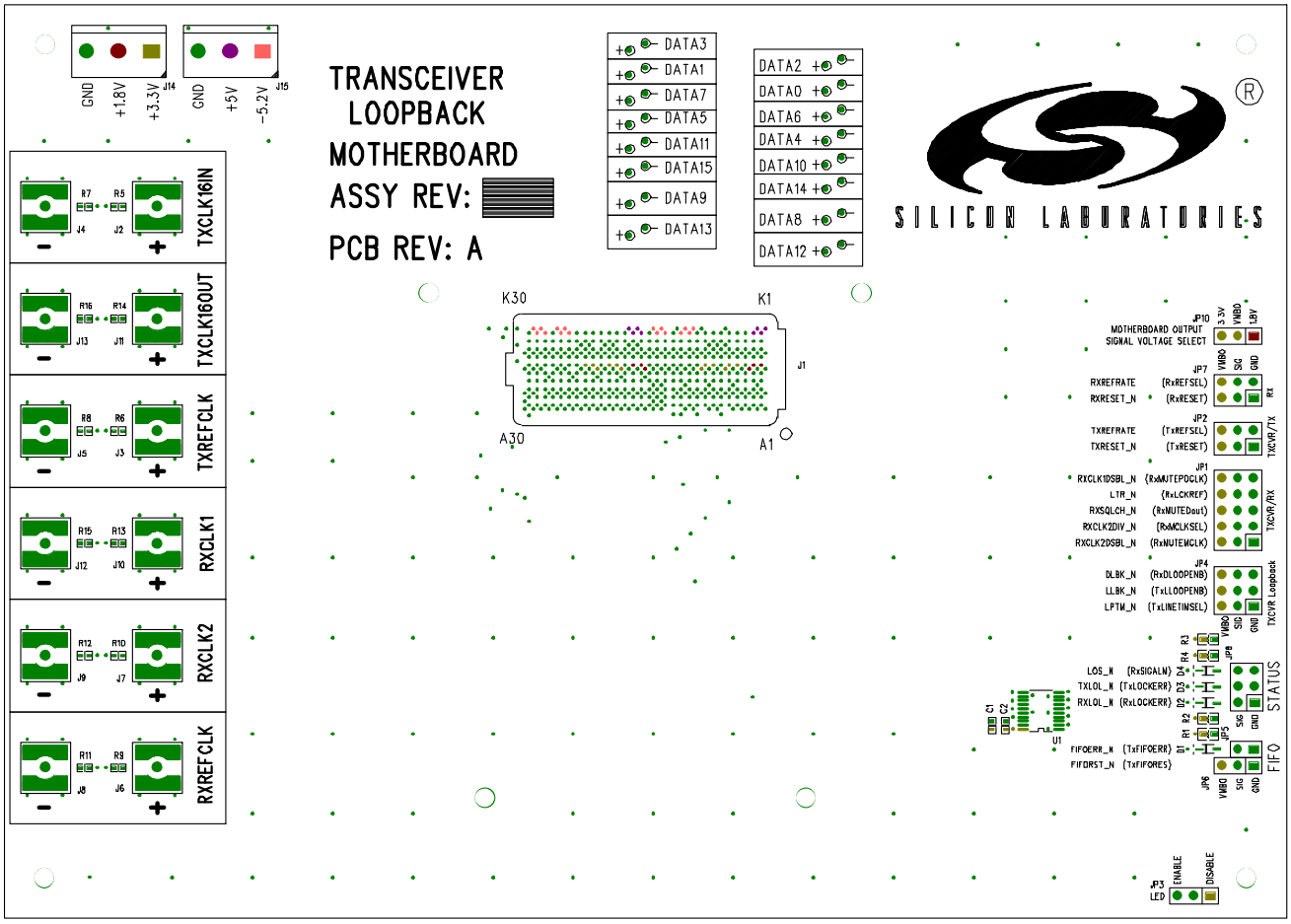



**Figure 38. Component Side Assembly (Loopback Motherboard)**

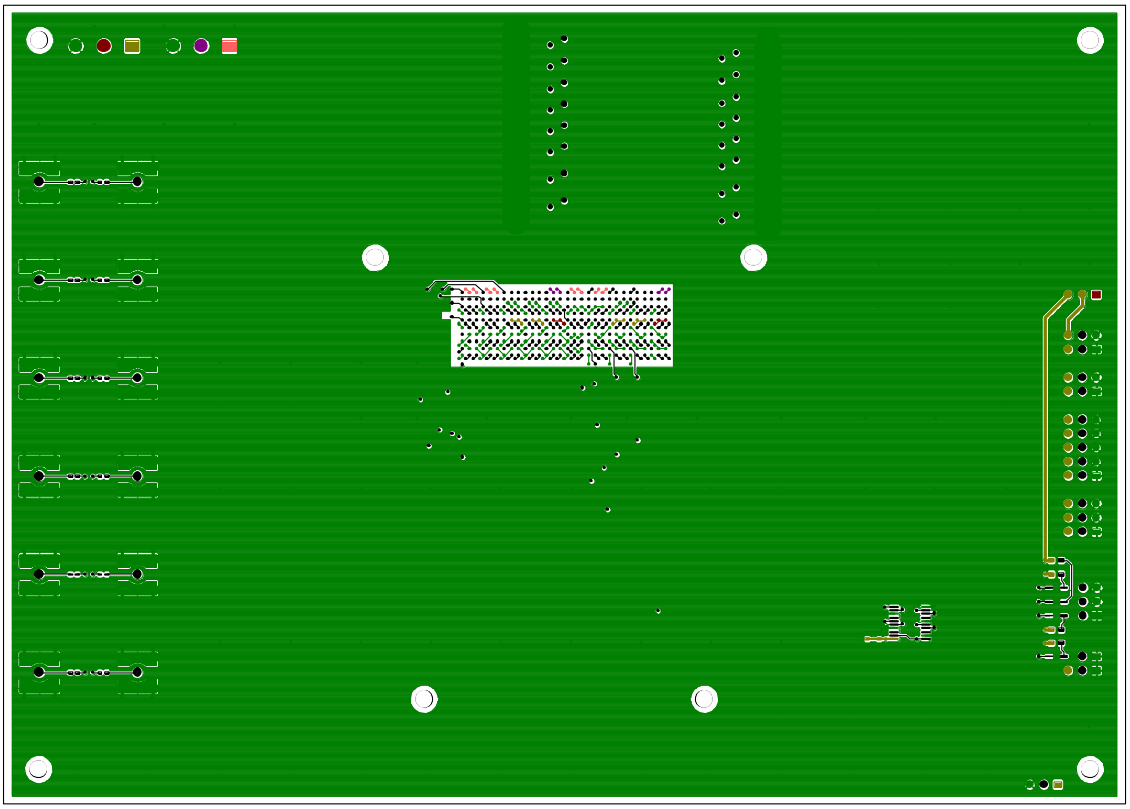


Figure 39. Layer 1—Component Side (Loopback Motherboard)

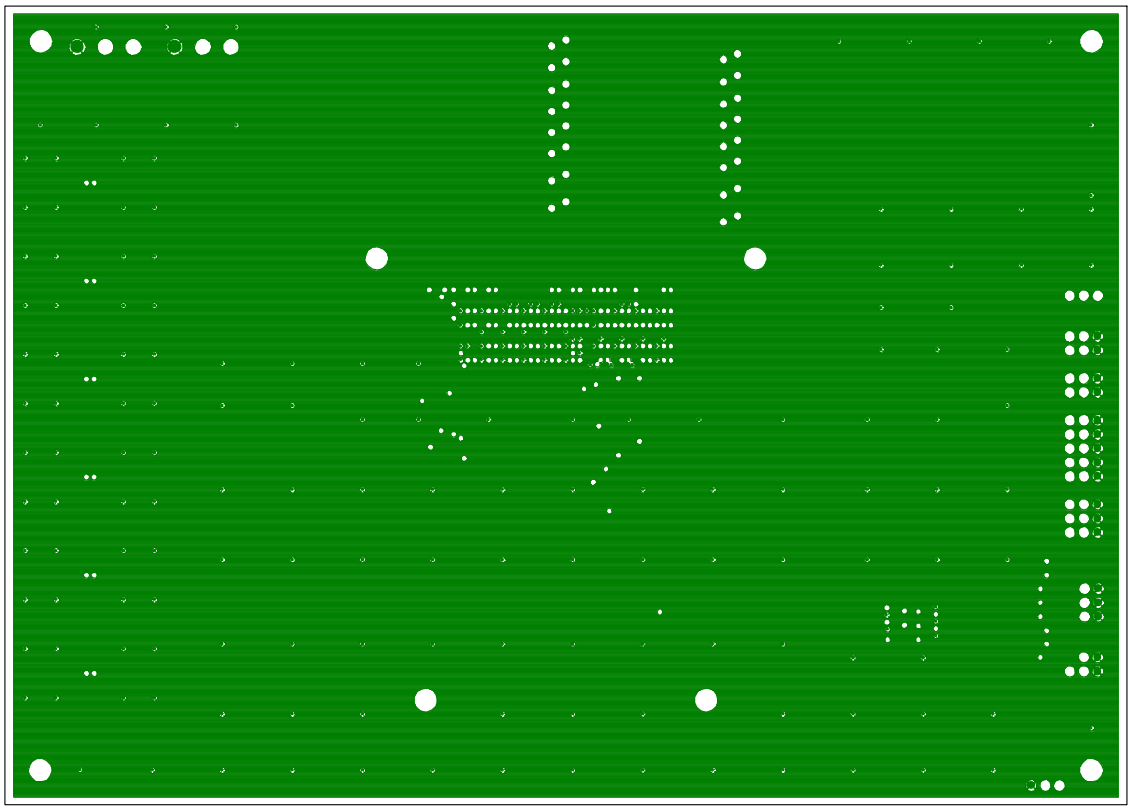


**Figure 40. Layer 2—GND1 Plane (Loopback Motherboard)**

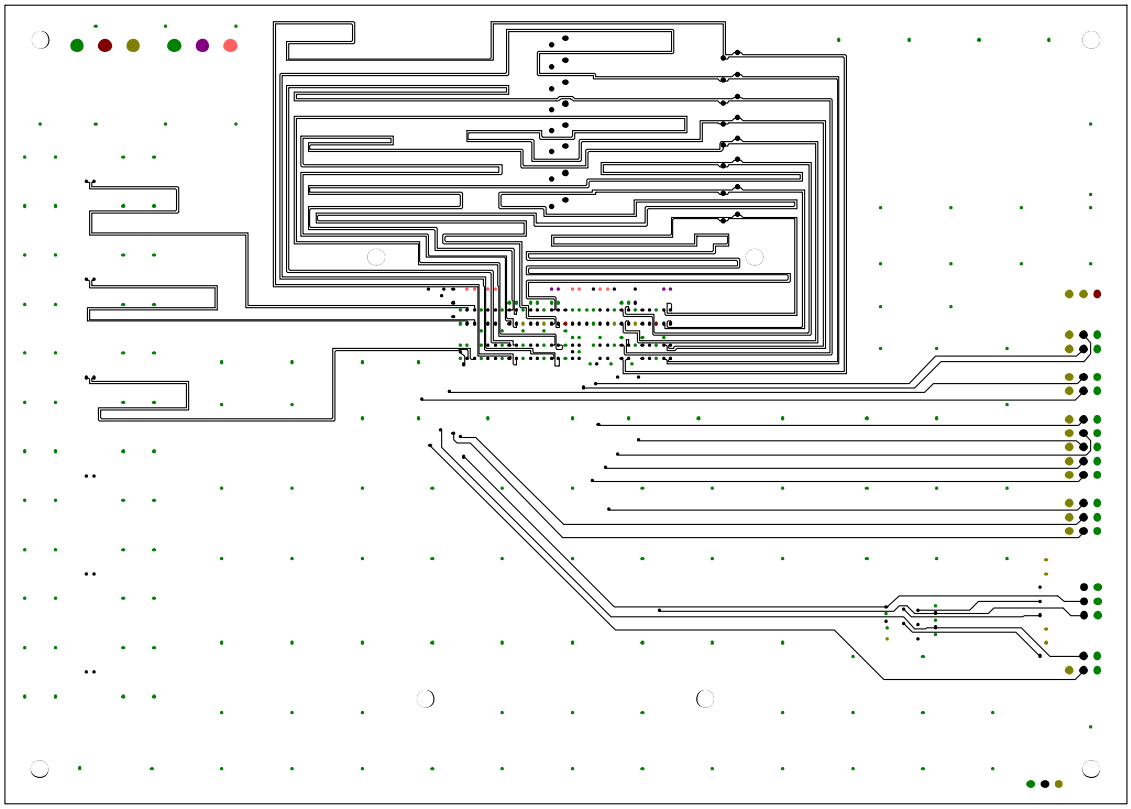


**Figure 41. Layer 3—Signal 1 Plane (Loopback Motherboard)**

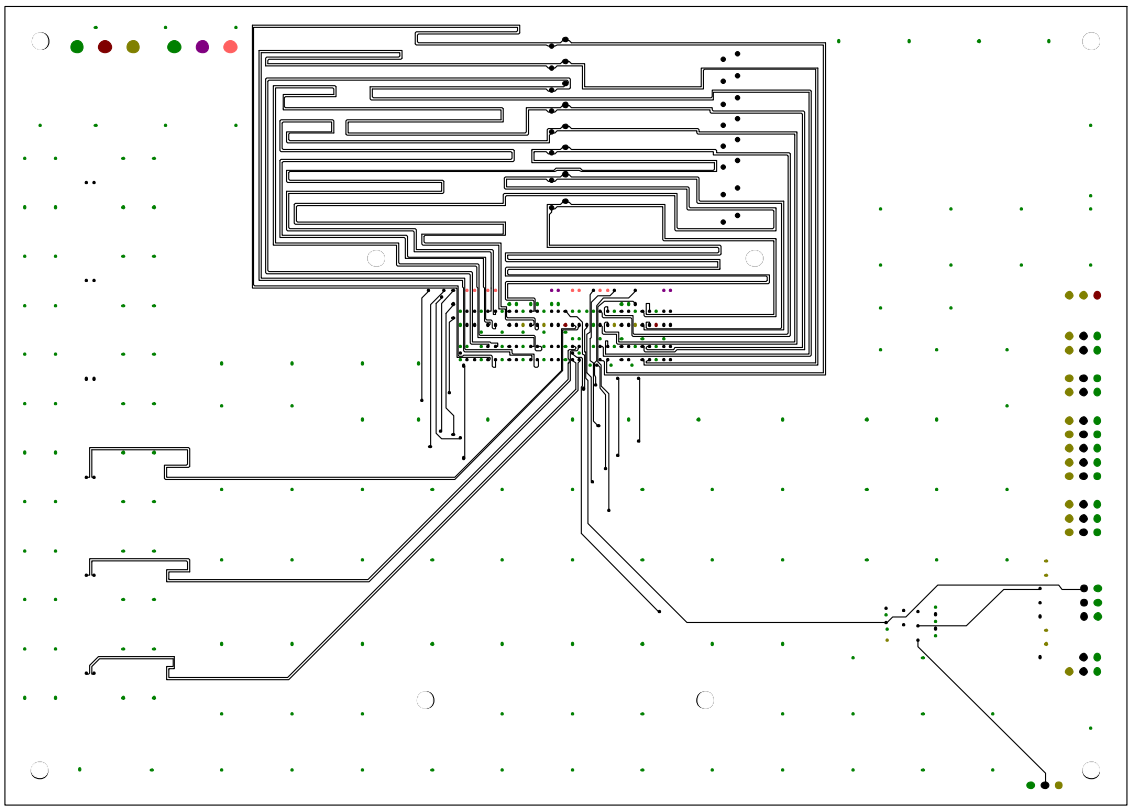


**Figure 42. Layer 4—Signal 2 Plane (Loopback Motherboard)**

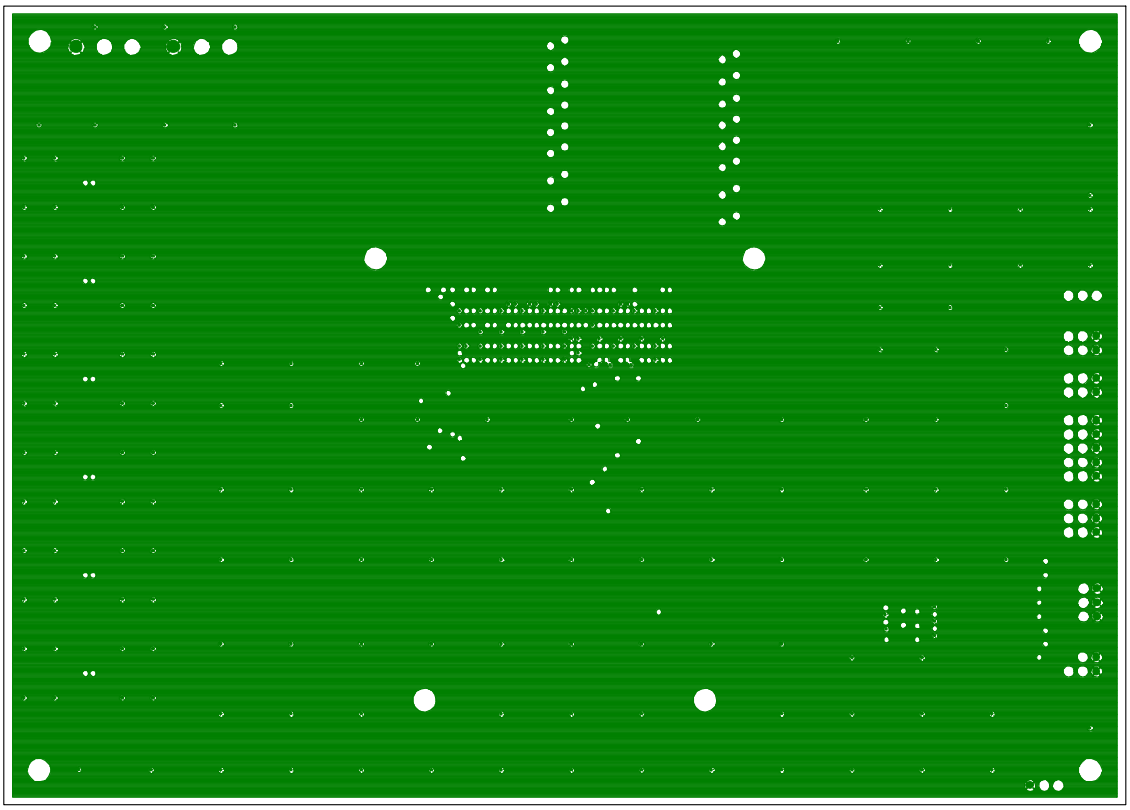


**Figure 43. Layer 5—GND2 Plane (Loopback Motherboard)**

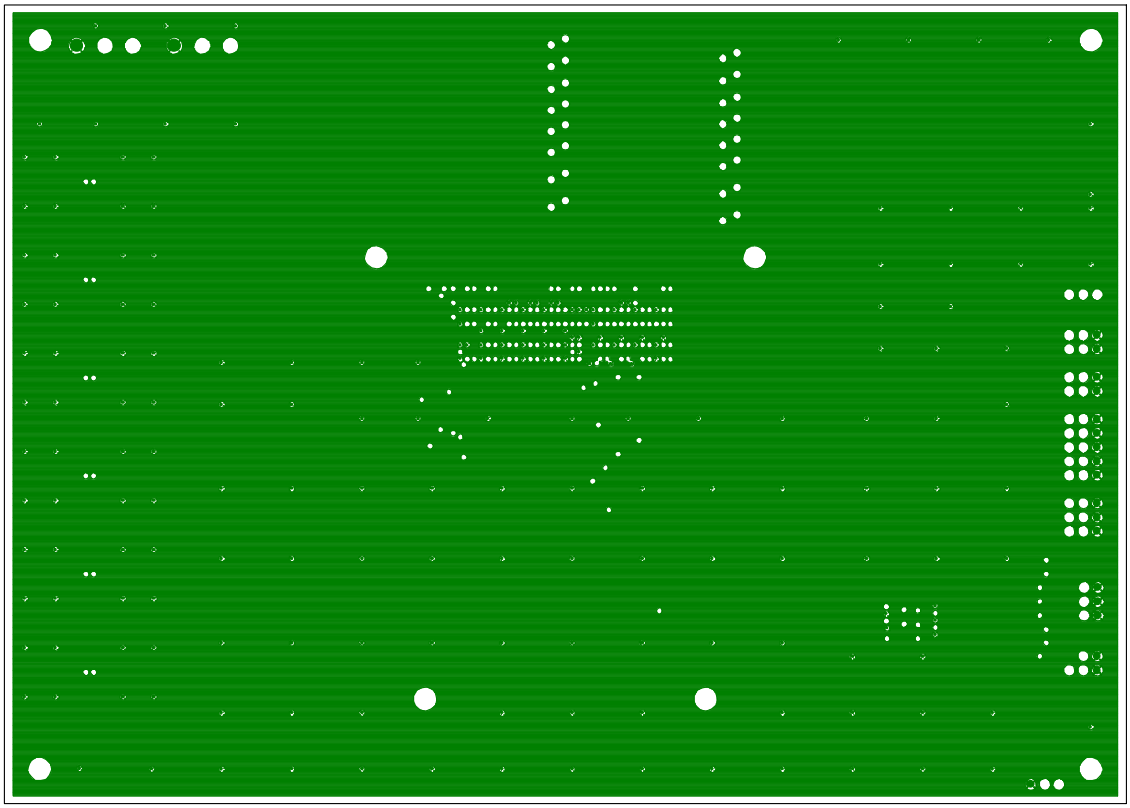


**Figure 44. Layer 6—Solder Side (Loopback Motherboard)**

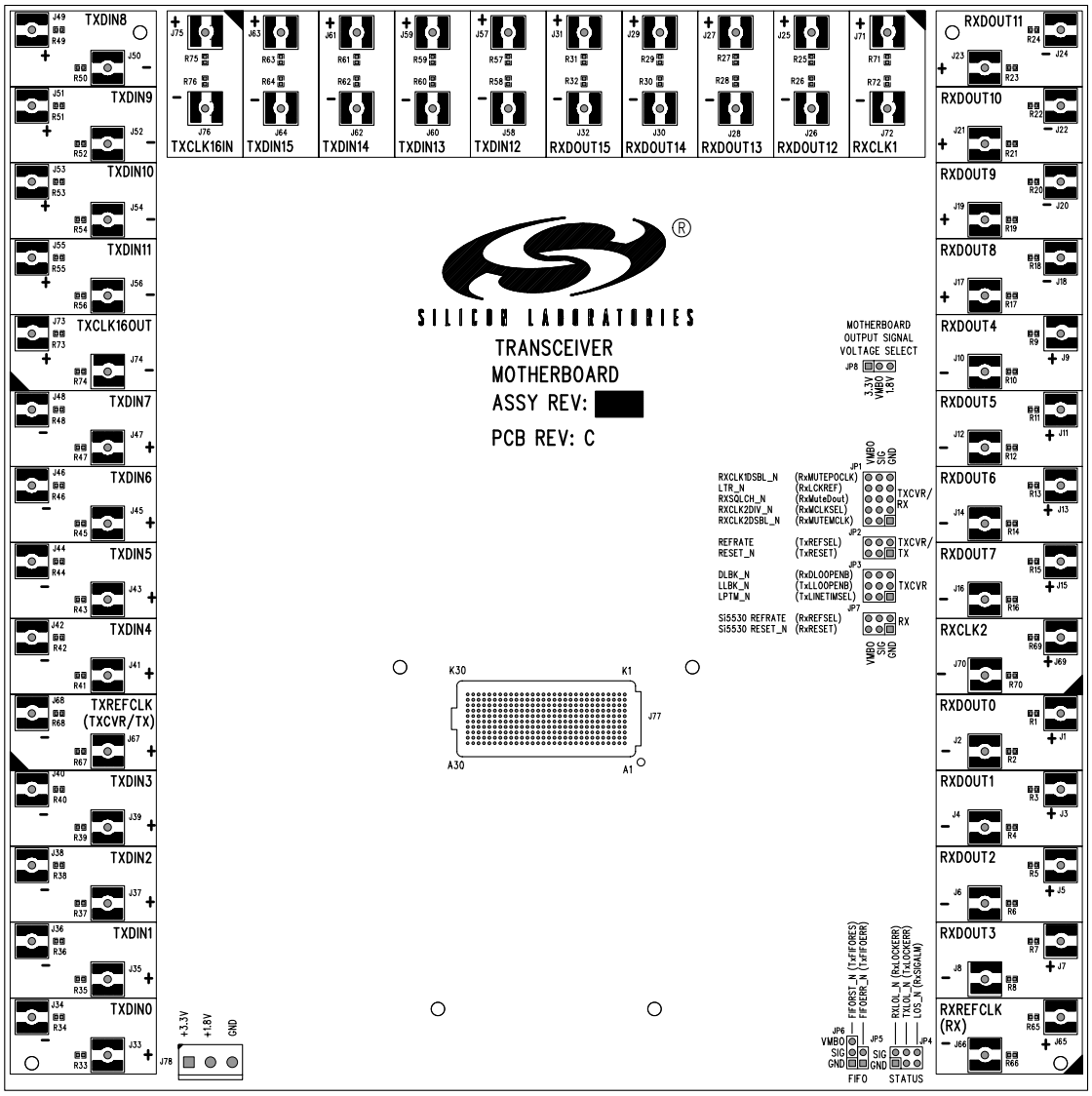



**Figure 45. Component Side Assembly (Optional Full-Duplex Motherboard)**

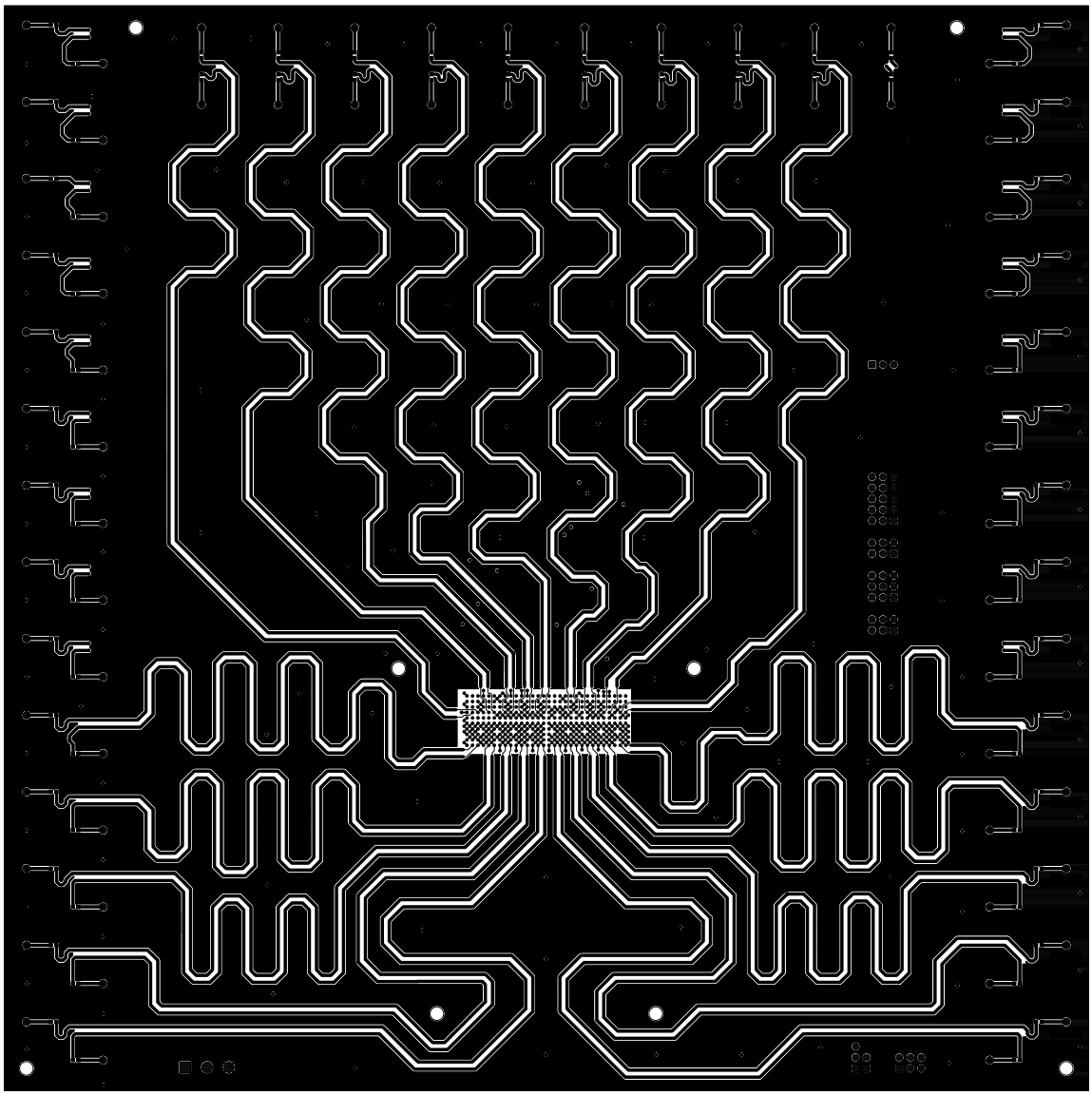


**Figure 46. Layer 1—Component Side (Optional Full-Duplex Motherboard)**

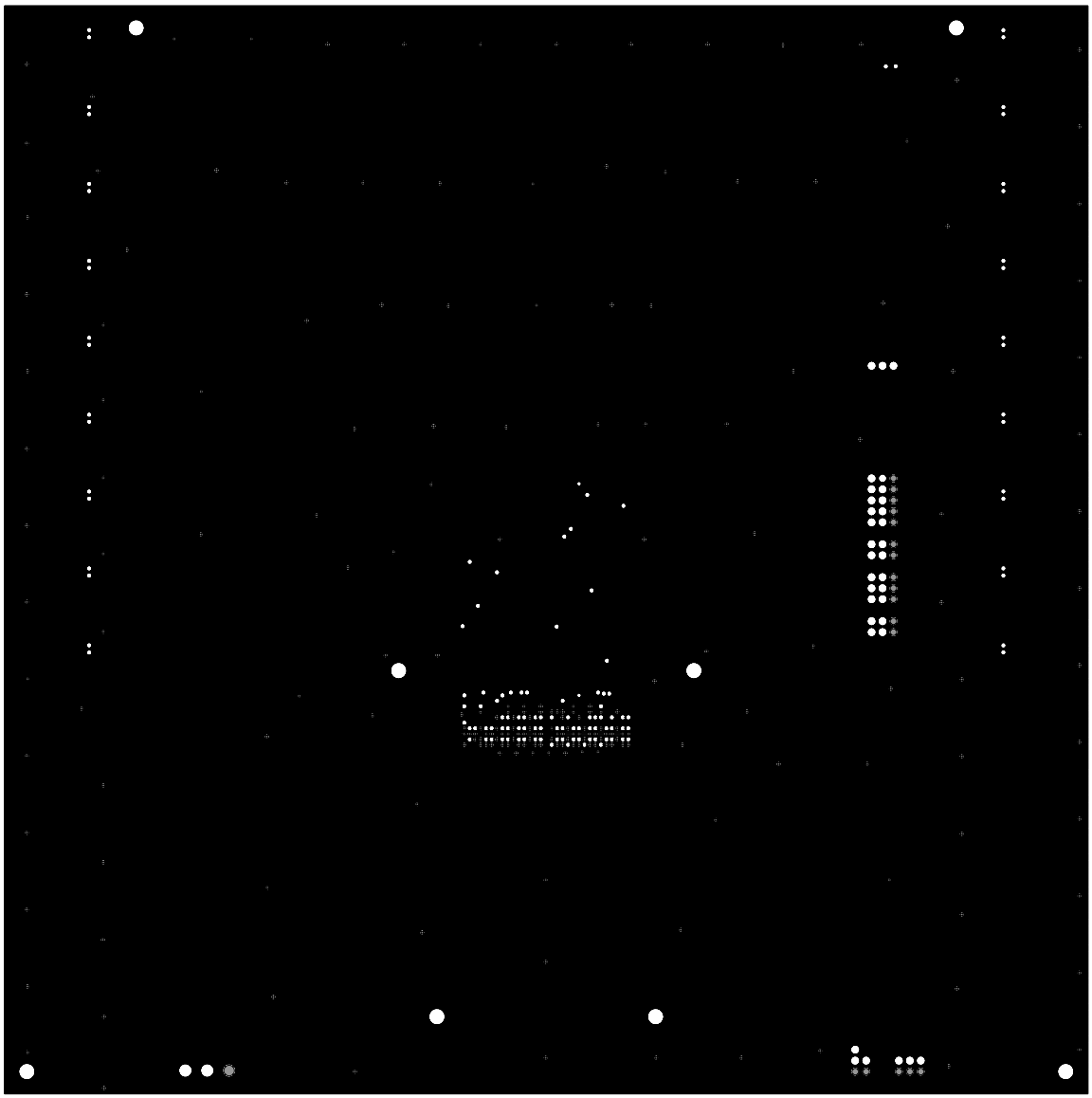


**Figure 47. Layer 2—GND1 Plane (Optional Full-Duplex Motherboard)**

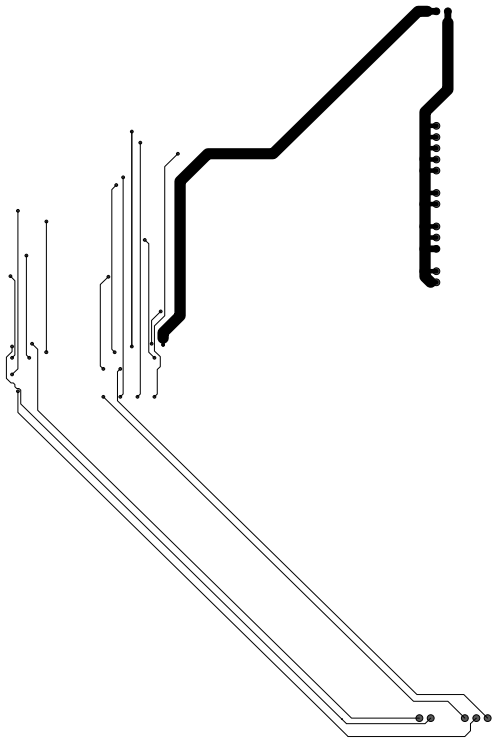


**Figure 48. Layer 3—Signal 1 Plane (Optional Full-Duplex Motherboard)**

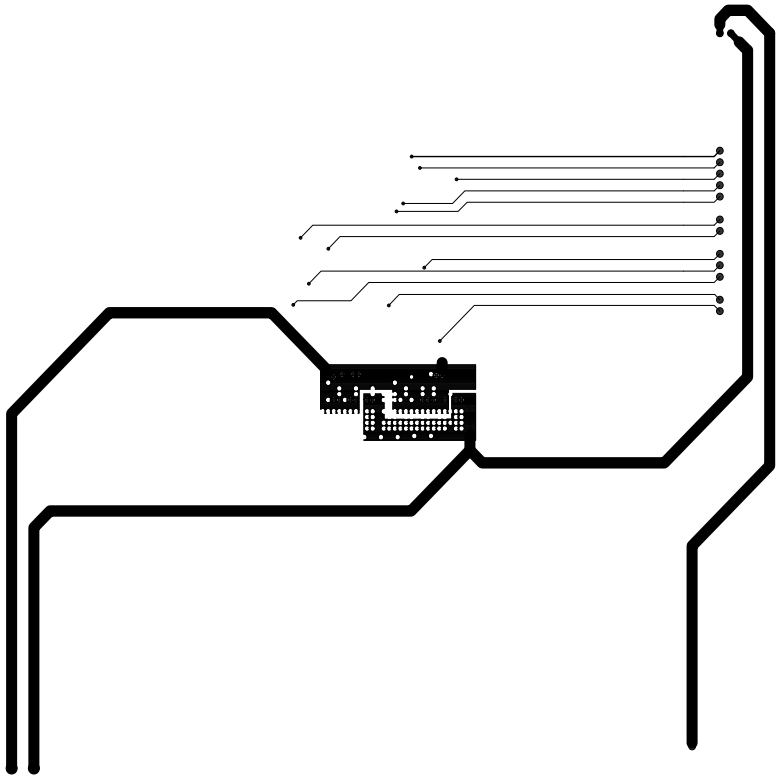


**Figure 49. Layer 4—Signal 2 Plane (Optional Full-Duplex Motherboard)**

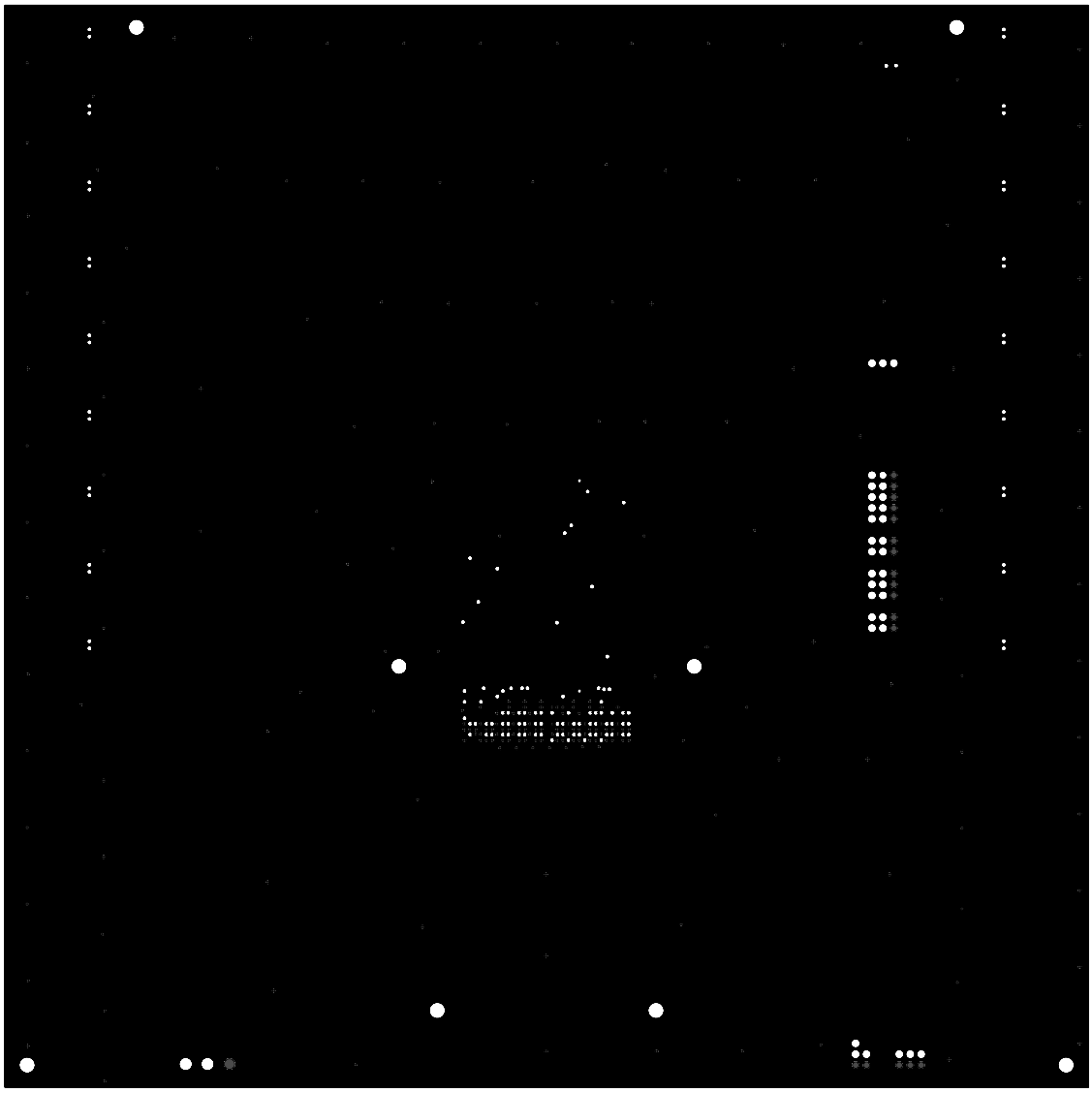


**Figure 50. Layer 5—GND2 Plane (Optional Full-Duplex Motherboard)**

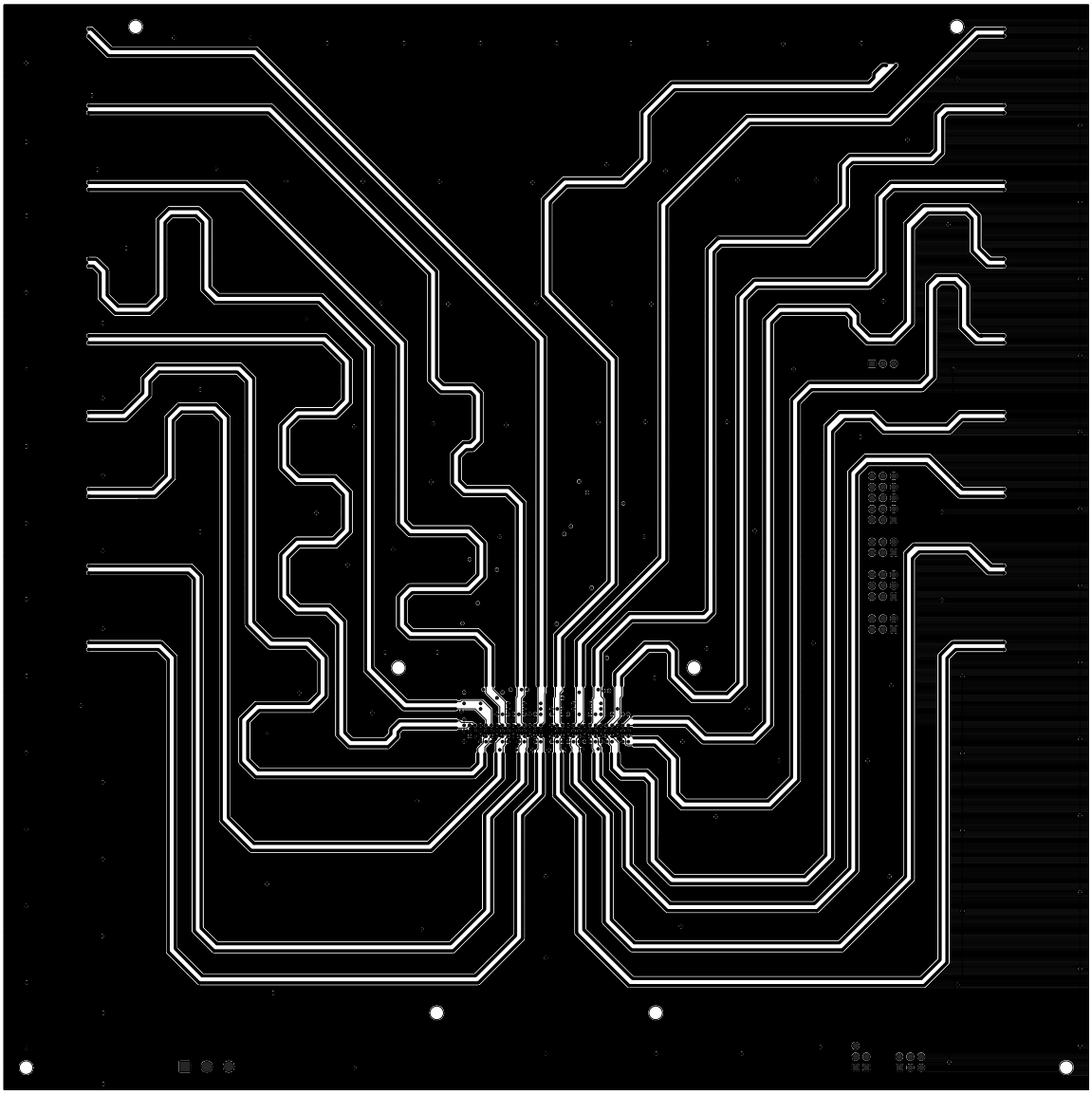


**Figure 51. Layer 6—Solder Side (Optional Full-Duplex Motherboard)**

# Document Change List

## Revision 0.4 to Revision 0.5

- Split Table 3 into Tables 3 and 4 to reflect differences in the actual PCBs for the Si5100 and Si5110 devices.
- Updated table references to reflect the changes in Table 3 and the creation of Table 4.

# Evaluation Board Assembly Revision History

### Si5100-EVB Daughter Card Revision History

| Assembly Level | PCB | Si5600 Device | Assembly Notes |
|---|---|---|---|
| C-01 | Rev. B | Rev. C | Assemble per BOM rev C-01 |
| D-01 | Rev. B | Rev. D | Assemble per BOM rev D-01 |

### Full-Duplex Motherboard Revision History

| Assembly Level | PCB | Assembly Notes |
|---|---|---|
| A-01 | Rev. A | Assemble per BOM rev A-01 |
| B-01 | Rev. B | Assemble per BOM rev B-01 |
| C-01 | Rev. C | Assemble per BOM rev C-01 |

### Loopback Motherboard Revision History

| Assembly Level | PCB | Assembly Notes |
|---|---|---|
| A-01 | Rev. A | Assemble per BOM rev A-01 |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