Dual 800mA/400mA, 1.2MHz/2.2MHz Synchronous Step-Up DC/DC Converters

FEATURES

- **Dual Synchronous Step-Up DC/DC Converters**
- **Delivers 3.3V at 200mA/100mA from one Alkaline/ NiMH Cell, or 3.3V at 400mA/200mA from Two Cells**
- **V_{IN} Start-Up Voltage: 700mV**
- **0.5V to 5V V_{IN} Range After Start-Up**
- **1.6V to 5.25V V_{OUT} Range**
- **Output Disconnect in Shutdown**
- **$V_{IN} > V_{OUT}$ Operation**
- **1.2MHz or 2.2MHz Operation**
- **Up to 94% Efficiency**
- 12µA Quiescent Current in Burst Mode® Operation
- Inrush Current Limiting and Soft-Start
- Internal Synchronous Rectifiers
- Logic-Controlled Shutdown (< 2µA)
- Quick V_{OUT} Discharge (LTC3527-1)
- 16-Lead, 0.75mm × 3mm × 3mm QFN Package

APPLICATIONS

- MP3/Personal Media Players
- Noise Canceling/Bluetooth Headsets
- Wireless Mice
- Portable Medical Instruments

DESCRIPTION

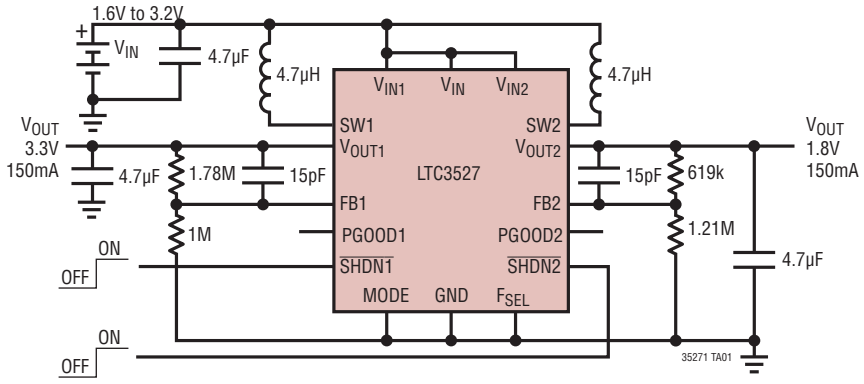
The LTC®3527/LTC3527-1 are dual high efficiency, step-up DC/DC converters in a space saving 16-lead 3mm × 3mm QFN package. Battery life is maximized with a 700mV start-up voltage and operation down to 500mV once started. The $\overline{SHDN}$ and PGOOD pins enable the converters to be sequenced or started together.

The LTC3527/LTC3527-1 limit inrush current during start-up. Selectable 1.2MHz or 2.2MHz operation provides a choice between the highest efficiency or smallest solution footprint. The current mode PWM design is internally compensated reducing external parts count. Burst Mode operation or fixed frequency operation is selectable via the MODE pin. Anti-ring circuitry reduces EMI in discontinuous mode. This device also features thermal shutdown.

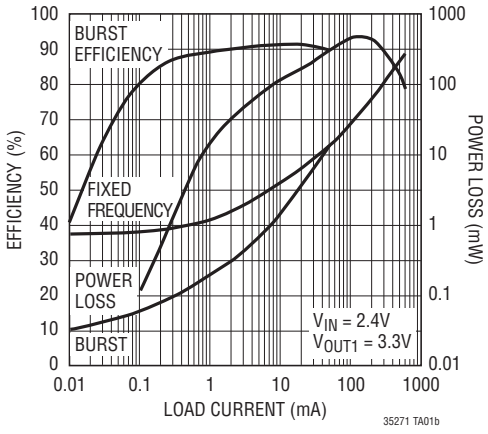
True output disconnect allows the output to be completely open in shutdown. The LTC3527-1 actively discharges V_{OUT1} or V_{OUT2} when its respective $\overline{SHDN}$ goes low. Quiescent current in shutdown is less than 2µA.

TYPICAL APPLICATION

Two-Cell Alkaline to 3.3V/1.8V Synchronous Boost Converters



1.2MHz Efficiency and Power Loss

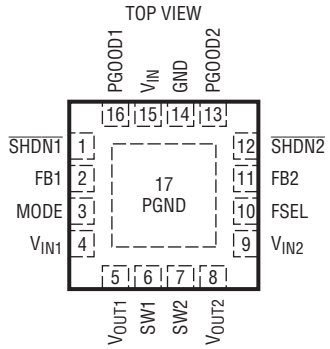


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{IN1}, V_{IN2} Voltage .....–0.3V to 6V
SW1, SW2 Voltage (DC) .....–0.3V to 6V
(Pulsed < 100ns) .....–0.3V to 7V
$\overline{SHDN1}$, $\overline{SHDN2}$, FB1, FB2 Voltage.....–0.3V to 6V
V_{OUT1}, V_{OUT2}.....–0.3V to 6V
MODE, FSEL, PGOOD1, PGOOD2.....–0.3V to 6V
Operating Temperature (Notes 2, 5).....–40°C to 85°C
Junction Temperature .....125°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3527EUD#PBF	LTC3527EUD#TRPBF	LDDK	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC3527EUD-1#PBF	LTC3527EUD-1#TRPBF	LCXP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3527EUD	LTC3527EUD#TR	LDDK	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC3527EUD-1	LTC3527EUD-1#TR	LCXP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C to 85°C. V_{IN} = V_{IN1} = V_{IN2} = 1.2V, V_{OUT1} = V_{OUT2} = 3.3V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	I_{LOAD} = 1mA			0.7	0.88	V
Output Voltage Adjust Range	V_{OUT1} V_{OUT1} V_{OUT2} V_{OUT2}	● ● 	1.7 1.6 1.7 1.6		5.25 5.25 5.25 5.25	V V V V
Line Regulation	V_{IN} = 1V to 5V			0.005		%/V
Feedback Voltage FB1, FB2		●	1.176	1.20	1.224	V
Feedback Input Current FB1, FB2	$V_{FB1,2}$ = 1.20V			1	50	nA
Quiescent Current: Shutdown	$V_{\overline{SHDN1}}$ = $V_{\overline{SHDN2}}$ = 0V, Not Including Switch Leakage, V_{OUT1} = V_{OUT2} = 0V			0.1	2	µA
Quiescent Current: Burst Mode Operation	Measured on V_{OUT}, V_{FB1} = V_{FB2} = 1.5V			12		µA
Quiescent Current: Active	V_{FB1} = V_{FB2} > 1.2V (Note 3)			500	900	µA
NMOS Switch Leakage Current (LTC3527)	$V_{SW1,2}$ = 5V, $\overline{SHDN1,2}$ = 0V			0.1	10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C to 85°C. $V_{IN} = V_{IN1} = V_{IN2} = 1.2V$, $V_{OUT1} = V_{OUT2} = 3.3V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PMOS Switch Leakage Current (LTC3527)	$V_{SW1,2} = 5V$, $V_{OUT1,2} = 0V$, $\overline{SHDN1,2} = 0V$			0.1	10	µA
NMOS and PMOS Combined Switch Leakage Current (LTC3527-1)	$V_{SW1,2} = 5V$, $V_{OUT1,2} = 0V$, $\overline{SHDN1,2} = 0V$ (Note 6)			0.2	20	µA
NMOS Switch On-Resistance, SW1				0.30		Ω
NMOS Switch On-Resistance, SW2				0.50		Ω
PMOS Switch On-Resistance, SW1				0.40		Ω
PMOS Switch On-Resistance, SW2				0.60		Ω
NMOS Current Limit, SW1		●	800			mA
NMOS Current Limit, SW2		●	400			mA
Current Limit Delay to Output Time	(Note 4)			60		ns
Maximum Duty Cycle	$V_{FB1,2} = 1V$	●	85	90		%
Minimum Duty Cycle	$V_{FB1,2} = 1.3V$	●			0	%
Switching Frequency	$V_{FSEL} = 0V$	●	0.9	1.2	1.5	MHz
Switching Frequency	$V_{FSEL} = 3.3V$	●	1.8	2.2	2.8	MHz
$\overline{SHDN1,2}$ Input High Voltage			0.88			V
$\overline{SHDN1,2}$ Input Low Voltage					0.35	V
$\overline{SHDN1,2}$ Input Current	$V_{\overline{SHDN1,2}} = 3.3V$			1	2	µA
PGOOD1, PGOOD2 Threshold	Referenced to the Feedback Voltage		–6	–9	–14	%
PGOOD1, PGOOD2 Low Voltage	$I_{PGOOD1,2} = 1mA$			0.1	0.2	V
PGOOD1, PGOOD2 Leakage Current	$V_{PGOOD1,2} = 5.25V$			0.01	1	µA
MODE Input High Voltage			1			V
MODE Input Low Voltage					0.35	V
MODE Input Current	$V_{MODE} = 3.3V$			1	2	µA
FSEL Input High Voltage			0.88			V
FSEL Input Low Voltage					0.35	V
FSEL Input Current	$V_{FSEL} = 3.3V$			1	2	µA
Soft-Start Time				0.5		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3527E/LTC3527E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current is measured into the V_{OUT} pin since the supply current is bootstrapped to the output. The current will reflect to the input supply by: $(V_{OUT}/V_{IN}) \bullet (1/\text{Efficiency})$. All switches are off.

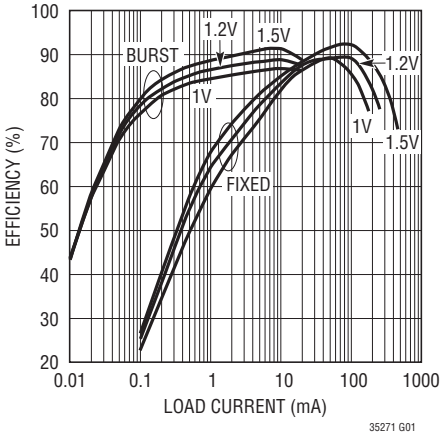
Note 4: Specification is guaranteed by design and not 100% tested in production.

Note 5: The LTC3527/LTC3527-1 includes an overtemperature shutdown that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when the overtemperature shutdown is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

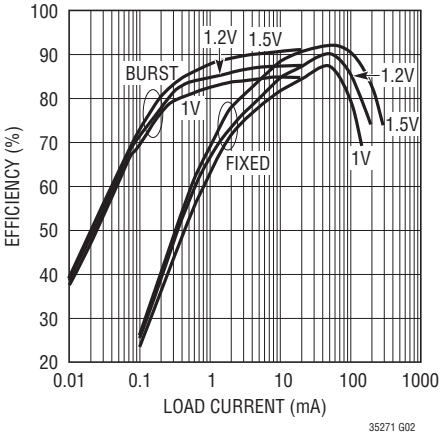
Note 6: The NMOS and PMOS switch leakage currents are tested in parallel for the LTC3527-1 because $V_{OUT1,2}$ are actively pulled to ground when $\overline{SHDN1,2} = 0V$

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

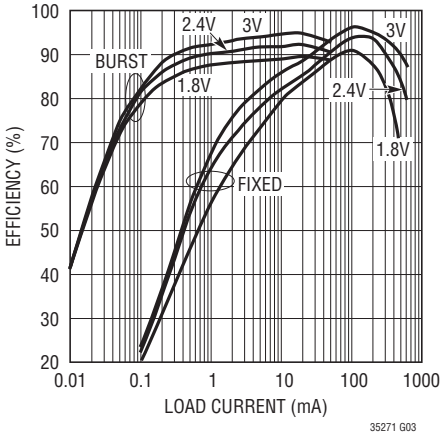
Efficiency vs Load Current and V_{IN} for V_{OUT1} = 1.8V at 1.2MHz



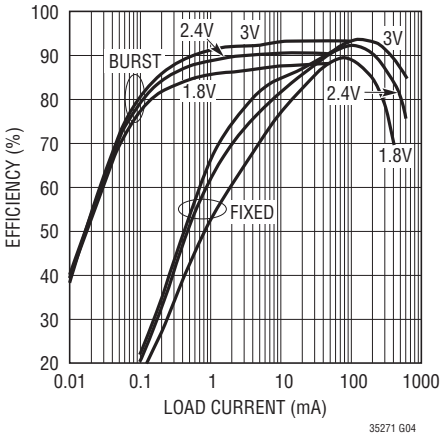
Efficiency vs Load Current and V_{IN} for V_{OUT2} = 1.8V at 1.2MHz



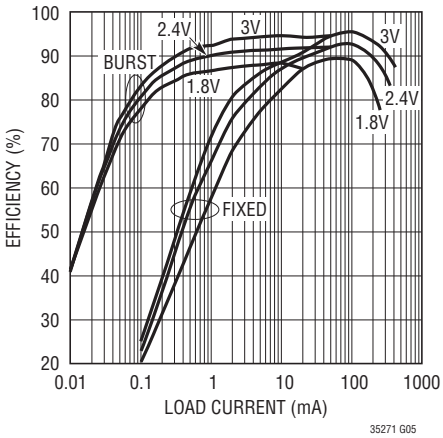
Efficiency vs Load Current and V_{IN} for V_{OUT1} = 3.3V at 1.2MHz



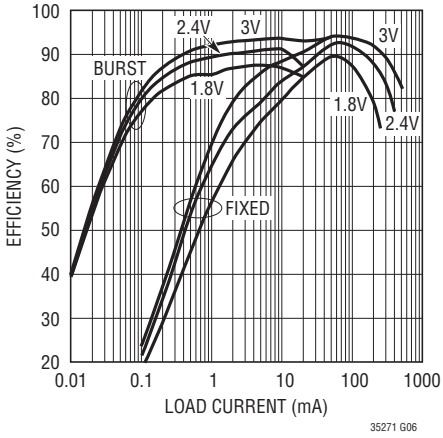
Efficiency vs Load Current and V_{IN} for V_{OUT1} = 3.3V at 2.2MHz



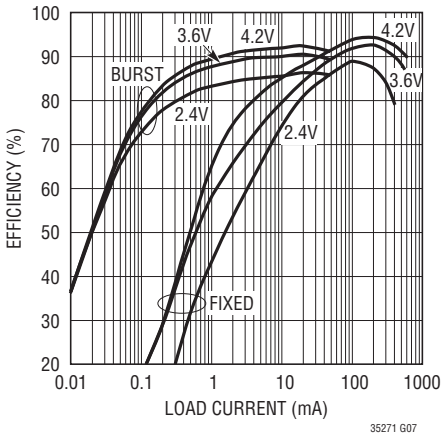
Efficiency vs Load Current and V_{IN} for V_{OUT2} = 3.3V at 1.2MHz



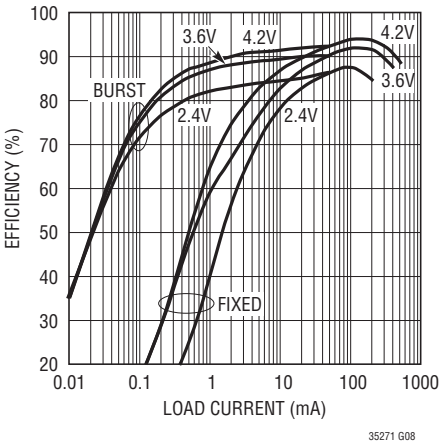
Efficiency vs Load Current and V_{IN} for V_{OUT2} = 3.3V at 2.2MHz



Efficiency vs Load Current and V_{IN} for V_{OUT1} = 5V at 1.2MHz

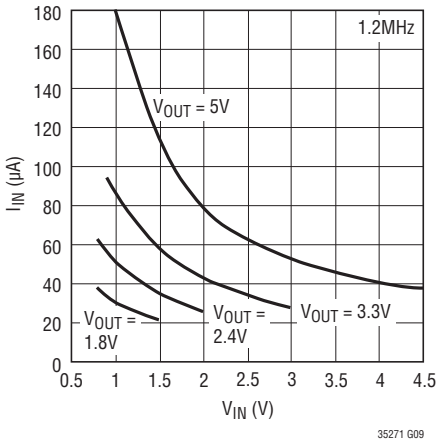


Efficiency vs Load Current and V_{IN} for V_{OUT2} = 5V at 1.2MHz

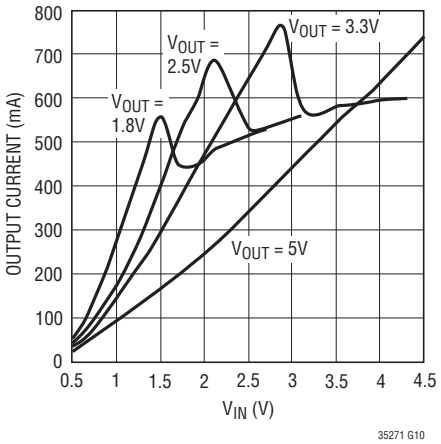


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

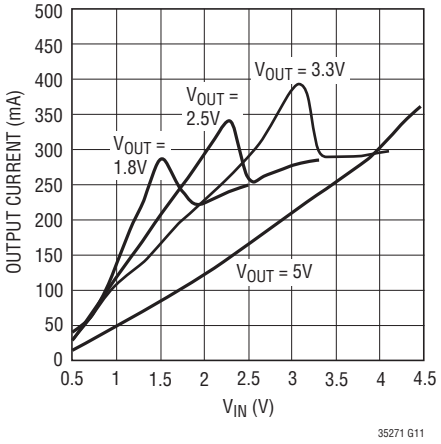
No-Load Input Current vs V_{IN}



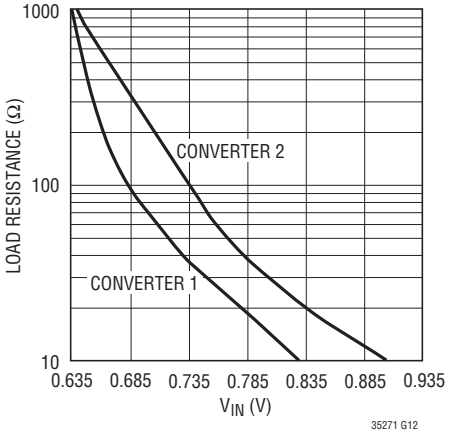
Maximum Output Current vs V_{IN} for Converter 1



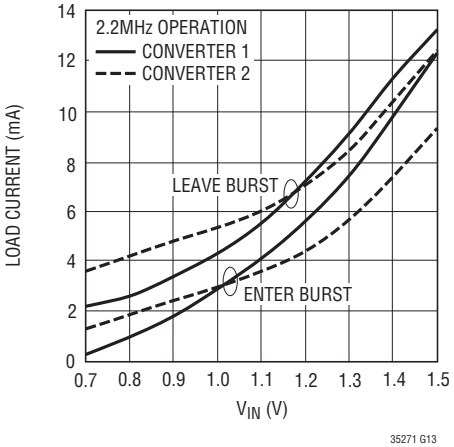
Maximum Output Current vs V_{IN} for Converter 2



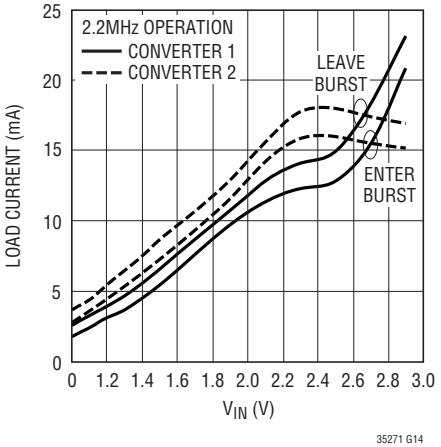
Minimum Load Resistance During Start-Up vs V_{IN}



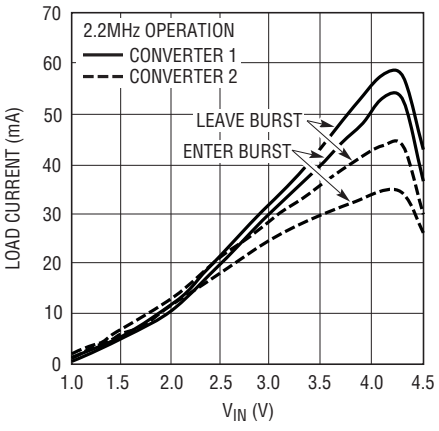
Burst Mode Threshold Current vs V_{IN} for V_{OUT1} = V_{OUT2} = 1.8V



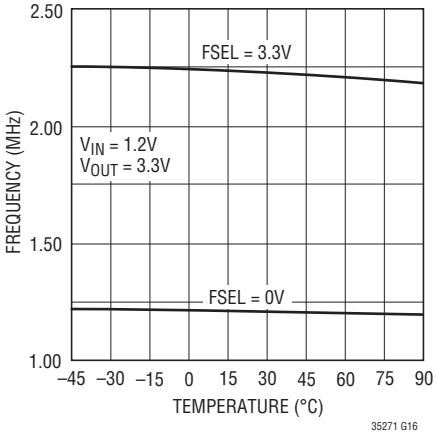
Burst Mode Threshold Current vs V_{IN} for V_{OUT1} = V_{OUT2} = 3.3V



Burst Mode Threshold Current vs V_{IN} for V_{OUT1} = V_{OUT2} = 5V

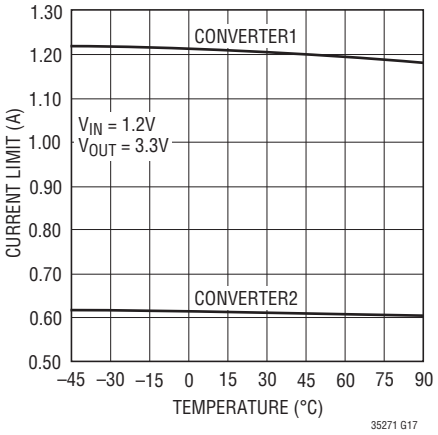


Oscillator Frequency vs Temperature

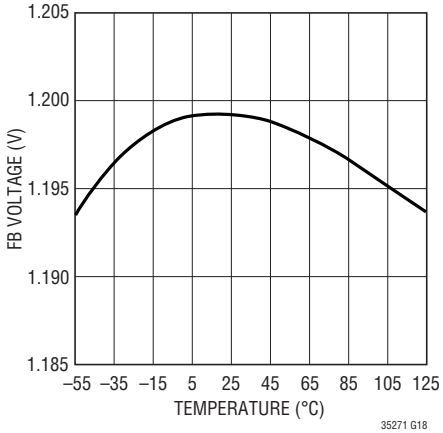


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

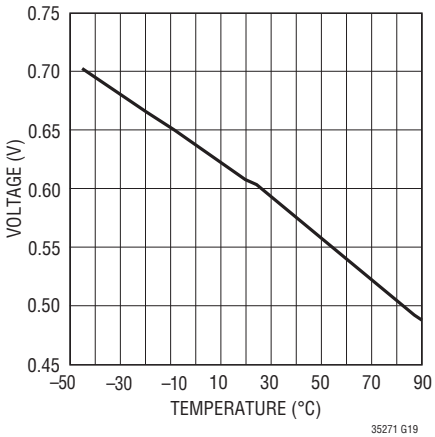
Current Limit vs Temperature



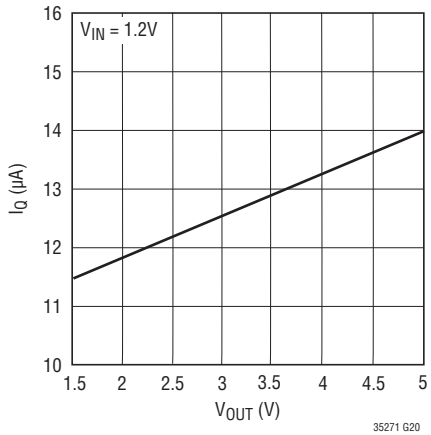
Feedback Voltage vs Temperature



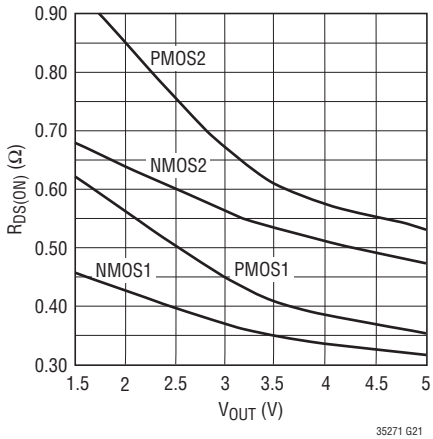
Start-Up Voltage vs Temperature



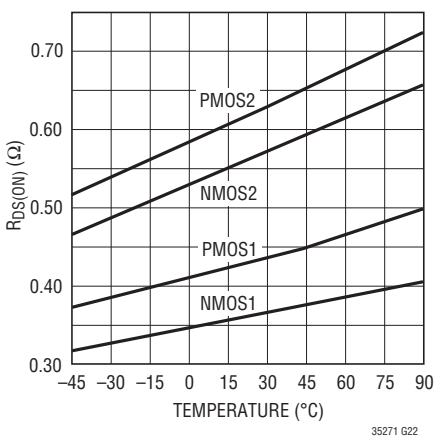
Burst Mode Quiescent Current vs V_{OUT}



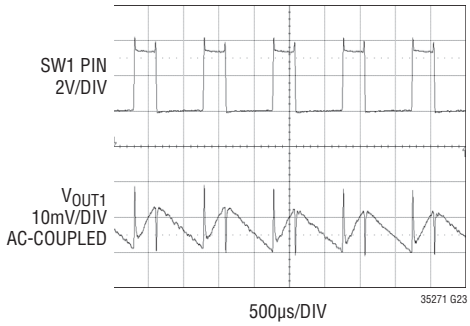
$R_{DS(ON)}$ (NMOS and PMOS) vs V_{OUT}



$R_{DS(ON)}$ (NMOS and PMOS) Change vs Temperature



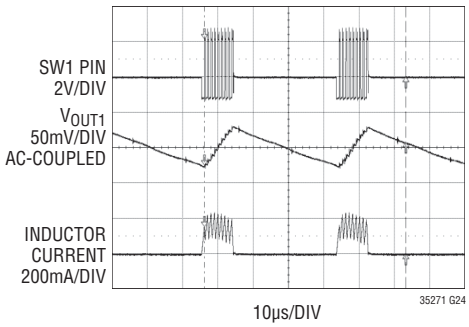
Fixed Frequency Switching Waveform and V_{OUT} Ripple



500µs/DIV

V_{IN1} = 1.2V
V_{OUT1} = 3.3V AT 100mA
C_{OUT1} = 10µF

Burst Mode Waveforms

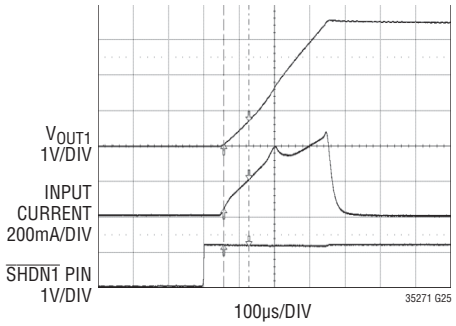


10µs/DIV

V_{IN1} = 1.2V
V_{OUT1} = 3.3V
C_{OUT1} = 10µF

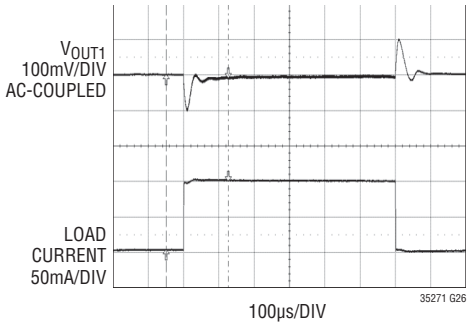
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

V_{OUT} and I_{IN} During Start-Up



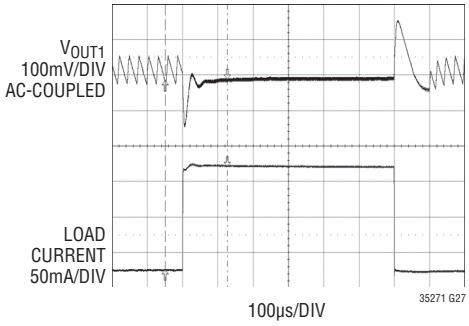
V_{OUT1} = 3.3V
C_{OUT1} = 10µF

V_{OUT1} Load Step Response Fixed Frequency at 1.2MHz



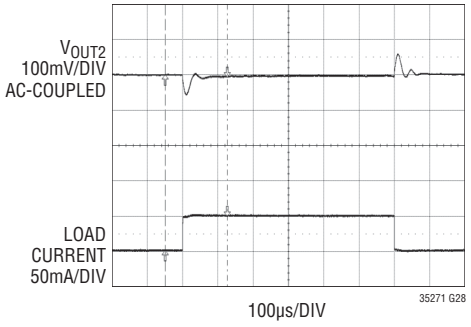
V_{IN} = 3.6V 50mA TO 150mA STEP
V_{OUT1} = 5V C_{OUT1} = 10µF

V_{OUT1} Load Step Response Burst Mode Operation at 1.2MHz



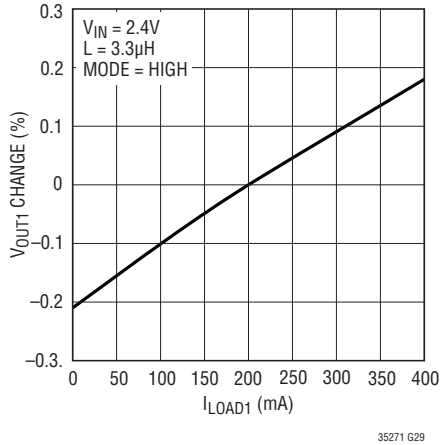
V_{IN} = 3.6V 20mA TO 170mA STEP
V_{OUT1} = 5V C_{OUT1} = 10µF

V_{OUT2} Load Step Response Fixed Frequency at 2.2MHz

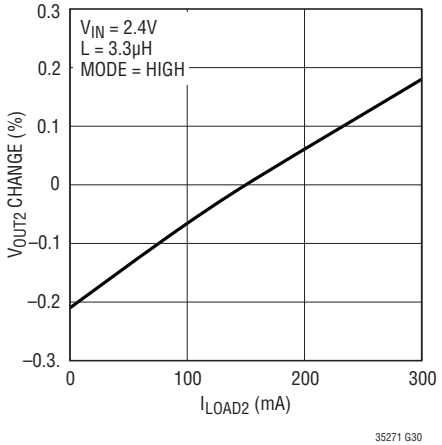


V_{IN} = 3.6V 50mA TO 100mA STEP
V_{OUT2} = 5V C_{OUT2} = 10µF

V_{OUT1} = 5V Load Regulation



V_{OUT2} = 3.3V Load Regulation



PIN FUNCTIONS

$\overline{SHDN1}$ (Pin 1): Boost Converter 1 Logic-Controlled Shutdown Input. There is an internal 4MΩ pull-down on this pin.

- $\overline{SHDN1}$ = High: Normal free running operation, 1.2MHz/2.2MHz typical operating frequency.
- $\overline{SHDN1}$ = Low: Shutdown, quiescent current < 2µA.

Note: Both converters must be shut down together to achieve < 2µA quiescent current.

FB1 (Pin 2): Boost Converter 1 Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.6V to 5.25V by:

$$V_{OUT1} = 1.20V \bullet \left[1 + \frac{R1}{R2}\right] \quad \text{(See Block Diagram)}$$

MODE (Pin 3): Logic-Controlled Mode Input for Both Boost Converters.

- MODE = High: Fixed frequency operation
- MODE = Low: Automatic Burst Mode operation

MODE pin must be 1V or greater to ensure fixed frequency over all operating conditions.

V_{OUT1} (Pin 5): Boost Converter 1 Output Voltage Sense Input and Drain of the Internal Synchronous Rectifier MOSFET. Driver bias is derived from V_{OUT1}. PCB trace length from V_{OUT1} to the output filter capacitor(s) should be as short and wide as possible.

SW1 (Pin 6): Boost Converter 1 Switch Pin. Connect the inductor between SW1 and V_{IN1}. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero or $\overline{SHDN1}$ is low, an internal 100Ω anti-ringing switch is connected from SW1 to V_{IN1} to minimize EMI.

SW2 (Pin 7): Boost Converter 2 Switch Pin. Connect the inductor between SW2 and V_{IN2}. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero or $\overline{SHDN2}$ is low, an internal 100Ω anti-ringing switch is connected from SW2 to V_{IN2} to minimize EMI.

V_{OUT2} (Pin 8): Boost Converter 2 Output Voltage Sense Input and Drain of the Internal Synchronous Rectifier MOSFET. Driver bias is derived from V_{OUT2}. PCB trace length from V_{OUT2} to the output filter capacitor(s) should be as short and wide as possible.

FSEL (Pin 10): Logic-Controlled Frequency Select Input.

- FSEL = High: 2.2MHz operation
- FSEL = Low: 1.2MHz operation

FB2 (Pin 11): Boost Converter 2 Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.6V to 5.25V by:

$$V_{OUT2} = 1.20V \bullet \left[1 + \frac{R3}{R4}\right] \quad \text{(See Block Diagram)}$$

$\overline{SHDN2}$ (Pin 12): Boost Converter 2 Logic-Controlled Shutdown Input. There is an internal 4MΩ pull-down on this pin.

- $\overline{SHDN2}$ = High: Normal free-running operation, 1.2MHz/2.2MHz typical operating frequency.
- $\overline{SHDN2}$ = Low: Shutdown, quiescent current < 2µA.

Note: Both converters must be shut down together to achieve < 2µA quiescent current.

PGOOD2 (Pin 13): Boost Converter 2 Power Good Comparator Output. This open-drain output is low when V_{FB} is 9% below its regulation voltage.

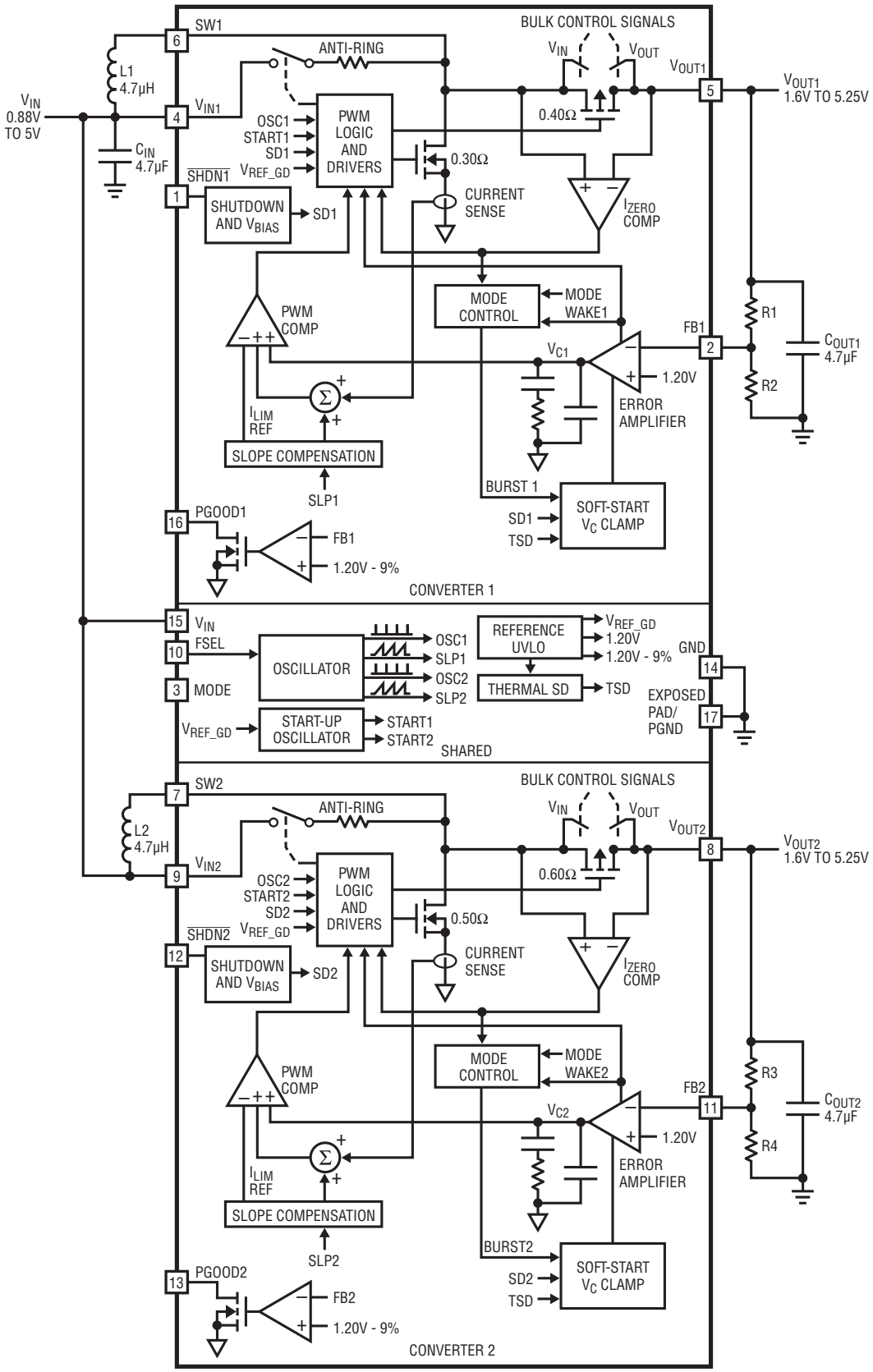
GND (Pin 14): Signal Ground. This pin is used as a ground reference for the internal circuitry of the LTC3527/LTC3527-1.

V_{IN}, V_{IN1}, V_{IN2} (Pins 15, 4, 9): Battery Input Voltage. See Operation section for more information.

PGOOD1 (Pin 16) Boost Converter 1 Power Good Comparator Output. This open-drain output is low when V_{FB} is 9% below its regulation voltage.

PGND (Exposed Pad Pin 17): Backplane. The exposed pad is PGND and must be soldered to the PCB ground plane. It serves as the power ground connection for V_{OUT1} and V_{OUT2}, and as a means of conducting heat away from the package.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC3527/LTC3527-1 are dual 1.2MHz/2.2MHz synchronous boost converters housed in a 16-lead 3mm × 3mm QFN package. With the ability to start up and operate from inputs less than 880mV, these devices feature fixed frequency, current mode PWM control for exceptional line and load regulation. The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components. Each converter has a separate input supply pin and is operated independently of the other, but they share the same oscillator thus providing in-phase switching. *If different input supply voltages are used, the third V_{IN} pin must be wired to the higher of the two supplies and each V_{OUT} must be higher than the highest V_{IN}.* Bypass capacitors are recommended on all V_{IN} pins.

With low $R_{DS(ON)}$ and low gate charge internal N-channel MOSFET switches and P-channel MOSFET synchronous rectifiers, the LTC3527/LTC3527-1 achieve high efficiency over a wide range of load current. With the MODE pin low, automatic Burst Mode operation maintains high efficiency at very light loads, reducing the quiescent current to just 12µA. If MODE is high, fixed frequency PWM switching provides low voltage ripple on the outputs. Operation can be best understood by referring to the Block Diagram.

A PGOOD signal is provided independently for each converter which can be used with the $\overline{SHDN}$ pins to provide sequencing of the outputs.

The LTC3527-1 provides an instant off feature which discharges V_{OUT1} or V_{OUT2} when their respective $\overline{SHDN}$ pins go low.

A frequency select function allows for 1.2MHz switching (FSEL = Low) or 2.2MHz switching (FSEL = High).

Low Voltage Start-Up

The LTC3527/LTC3527-1 include an independent start-up oscillator designed to start up at an input voltage of 0.7V (typical). The two converters can be started together or in either sequence of boost 1 and boost 2 with appropriate control of $\overline{SHDN1}$ and $\overline{SHDN2}$. Soft-start and inrush current limiting are provided to each converter independently during start-up, as well as during normal mode.

When V_{IN}, V_{OUT1}, or V_{OUT2} exceeds 1.4V (typical), the IC enters normal operating mode. Once the higher of V_{OUT1} or V_{OUT2} exceeds V_{IN} by 0.24V, the IC powers itself from the higher V_{OUT} instead of V_{IN}. At this point the internal circuitry has no dependency on the V_{IN} input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V.

With single-cell operation, the limiting factor for the application becomes the availability of the power source to supply sufficient energy to the outputs at low voltages, and maximum duty cycle, which is clamped at 90% (typical). Note that at low input voltages, small voltage drops due to the higher series resistance of a depleted cell become critical and greatly limit the power delivery capability of the converter. A higher value, low ESR input capacitor can help to improve this to a small degree.

Low Noise Fixed Frequency Operation

Soft-Start: The LTC3527/LTC3527-1 contain internal circuitry to provide independent soft-start operation to each converter. The soft-start circuitry ramps the peak inductor current from zero to its peak value of 900mA (typical) for converter 1 or 500mA (typical) for converter 2 in approximately 0.5ms, allowing start-up into heavy loads. The soft-start circuitry for both converters is reset in the event of a thermal shutdown or shutdown command.

Oscillator: An internal oscillator sets the switching frequency to 1.2MHz if the FSEL pin is below 0.35V, or 2.2MHz if the FSEL pin is above 0.88V.

Shutdown: Shutdown is accomplished independently for each converter by pulling its respective $\overline{SHDN}$ pin below 0.35V, and enabled by pulling each $\overline{SHDN}$ pin above 0.88V. Note that the $\overline{SHDN}$ pins can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than the absolute maximum rating.

Error Amplifier: The noninverting input of each transconductance error amplifier is internally connected to the 1.20V reference. The inverting inputs are connected

OPERATION

to FB1 for converter 1 and FB2 for converter 2. Clamps limit the minimum and maximum error amp output voltages for improved large-signal transient response. Power converter control loop compensation is provided internally. An external resistive voltage divider from V_{OUT1} (V_{OUT2}) to ground programs the respective output voltage via FB1 (FB2) from 1.6V to 5.25V.

$$V_{OUT1} = 1.20V \bullet \left[1 + \frac{R1}{R2}\right]$$

$$V_{OUT2} = 1.20V \bullet \left[1 + \frac{R3}{R4}\right] \quad \text{(See Block Diagram)}$$

Current Sensing: Lossless current sensing converts the peak current signal of each N-channel MOSFET switch into a voltage which is summed with its corresponding internal slope compensation. The summed signals are compared to their respective error amplifier outputs to provide individual peak current control commands for the PWM of each converter.

Current Limit: The current limit comparators shut off the N-channel MOSFET switches once their threshold is reached. Each current limit comparator delay time to output is typically 60ns. Peak switch current is limited to approximately 900mA for converter 1 and 500mA for converter 2, independent of input or output voltage. If V_{OUT1} or V_{OUT2} falls below 1V, its respective current limit is cut in half.

Zero Current Comparator: The zero current comparators monitor the inductor current to the outputs and shut off the synchronous rectifiers when the current reduces to approximately 30mA. This prevents the inductor current from reversing in polarity, improving efficiency at light loads.

Synchronous Rectifier: To control inrush current and to prevent the inductor currents from running away when V_{OUT1} or V_{OUT2} is close to V_{IN}, the P-channel MOSFET synchronous rectifiers are only enabled when their respective $V_{OUT} > (V_{IN} + 0.24V)$.

Anti-Ringing Control: The anti-ringing control connects a resistor across the inductor to prevent high frequency ringing on the SW1 (SW2) pins during discontinuous current mode operation. Although the ringing of the resonant circuit formed by the inductors and C_{SW} (capacitance on SW1 or SW2 pins) is low energy, it can cause EMI radiation.

Output Disconnect: The LTC3527/LTC3527-1 are designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifiers. This allows V_{OUT1} and V_{OUT2} to go to zero volts during shutdown, drawing no current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there must not be external Schottky diodes connected between the SW1 (SW2) pins and V_{OUT1} (V_{OUT2}). The output disconnect feature also allows V_{OUT1} or V_{OUT2} to be pulled high, without any reverse current into a battery on V_{IN}.

Thermal Shutdown: If the die temperature exceeds 160°C, the device will go into thermal shutdown. All switches will be turned off and the soft-start capacitors will be discharged. The device will be enabled again when the die temperature drops by about 15°C.

Burst Mode Operation

To realize the efficiency benefits of Burst Mode operation, both V_{OUT1} and V_{OUT2} must be under a light load current condition, if they are both enabled. If one converter is shut down, then Burst Mode operation is enabled on the other converter. With the MODE pin low, the LTC3527/LTC3527-1 will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode when the load increases. Refer to the Typical Performance Characteristics to see the Output Load Burst Mode Threshold Current vs V_{IN}. The load current at which Burst Mode operation is entered can be changed by adjusting the inductor value. Raising the inductor value will lower the load current at which Burst Mode is operation entered.

In Burst Mode operation, the LTC3527/LTC3527-1 still switch at a fixed frequency of 1.2MHz (FSEL = 0) or 2.2MHz (FSEL = 1), using the same error amplifier and loop compensation for peak current mode control. This control method eliminates the output transient when switching between modes. In Burst Mode operation, energy is delivered to the

OPERATION

output until it reaches the nominal regulation value, then the LTC3527/LTC3527-1 transition to sleep mode where the outputs are off and the LTC3527/LTC3527-1 consume only 12µA of quiescent current from the higher of V_{OUT1} or V_{OUT2}. When the output voltage droops slightly, switching resumes. This maximizes efficiency at very light loads by minimizing switching and quiescent current losses. Burst Mode output voltage ripple, which is typically 1% peak-to-peak, can be reduced by using more output capacitance (10µF or greater), or with a small capacitor (15pF) connected between V_{OUT1} (V_{OUT2}) and FB1 (FB2).

If either load current increases, the LTC3527/LTC3527-1 will automatically leave Burst Mode operation. Note that larger output capacitor values may cause this transition to occur at lighter loads. Once the LTC3527/LTC3527-1 have left Burst Mode operation and returned to normal operation, they will remain there until both output loads are reduced below the burst threshold current.

Burst Mode operation is inhibited during start-up and soft-start and until both V_{OUT1} and V_{OUT2} are at least 0.24V greater than V_{IN} if neither channel is in shutdown.

When the MODE pin is high, LTC3527/LTC3527-1 feature continuous PWM fixed frequency operation at 1.2MHz (FSEL = Low) or 2.2MHz (FSEL = High). At very light loads, the LTC3527/LTC3527-1 will exhibit pulse-skipping operation.

Single Cell to 5V Step-Up Applications

Due to the high inductor current slew rate in applications boosting to 5V from a single-cell (alkaline, NiCd or NiMH), the LTC3527/LTC3527-1 may not enter Burst Mode operation at input voltages below 1.5V in a 2.2MHz application (FSEL = high). For a single-cell to 5V application requiring Burst Mode 1.2MHz operation, (FSEL = low) is recommended. Refer to the Typical Performance Characteristics for the Burst Mode thresholds for different input and output voltages.

APPLICATIONS INFORMATION

$V_{IN} > V_{OUT}$ Operation

The LTC3527/LTC3527-1 will maintain output voltage regulation even when the input voltage is above one or both of the desired output voltages. Note, all V_{INS} must be common to support this mode of operation. Since this mode is less efficient and will dissipate more power in the LTC3527/LTC3527-1, the maximum output current capability is limited in order to maintain an acceptable junction temperature. When operating with $V_{IN} > V_{OUT}$ the power is defined by:

$$P_{OUT} = I_{OUT}\left[(V_{IN} + 1.5) - V_{OUT}\right]$$

To maintain a junction temperature below 125°C, the following formula must be adhered to:

$$(P_{OUT1} + P_{OUT2})\,68°C/W = 125 - T_A$$

where T_A is the ambient temperature.

Short-Circuit Protection

The LTC3527/LTC3527-1 output disconnect feature allows an output short-circuit while maintaining a maximum internally set current limit. The converters also incorporate internal features such as current limit foldback and thermal shutdown for protection from an excessive overload or short circuit. To reduce power dissipation under short-circuit conditions, the peak switch current limit is reduced to 500mA (typical) for converter 1 and 350mA (typical) for converter 2 when V_{OUT} is less than 1V.

Schottky Diode

Although it is not required, adding a Schottky diode from SW1 (SW2) to V_{OUT1} (V_{OUT2}) will improve efficiency by about 2%. Note that this defeats the output disconnect and short-circuit protection features.

APPLICATIONS INFORMATION

PCB Layout Guidelines

The high speed operation of the LTC3527/LTC3527-1 demands careful attention to board layout. A careless layout will result in reduced performance. Figure 1 shows the recommended component placement. A large ground pin copper area will help to lower the die temperature. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.

COMPONENT SELECTION

Inductor Selection

The LTC3527/LTC3527-1 can utilize small surface mount inductors due to their fast 1.2MHz/2.2MHz switching frequencies. Inductor values between 3.3µH and 4.7µH are suitable for most 1.2MHz applications. Inductor values between 1.5µH and 2.2µH are suitable for most 2.2MHz applications. Larger values of inductance will allow slightly greater output current capability (and lower the Burst Mode threshold) by reducing the inductor ripple current. Increasing the inductance above 10µH will increase size while providing little improvement in output current capability.

The minimum inductance value is given by:

$$L > \frac{V_{IN(MIN)} \bullet (V_{OUT(MAX)} - V_{IN(MIN)})}{f \bullet Ripple \bullet V_{OUT(MAX)}}$$

where:

Ripple = Allowable inductor current ripple (amps peak-to-peak)
$V_{IN(MIN)}$ = Minimum input voltage
$V_{OUT(MAX)}$ = Maximum output voltage
f = Oscillator frequency (MHz)

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the I^2R power losses, and must be able to support the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core area to support the peak inductor currents of 900mA (500mA) seen on the LTC3527/LTC3527-1. To minimize radiated noise, use shielded inductors. See Table 1 for suggested components and suppliers.

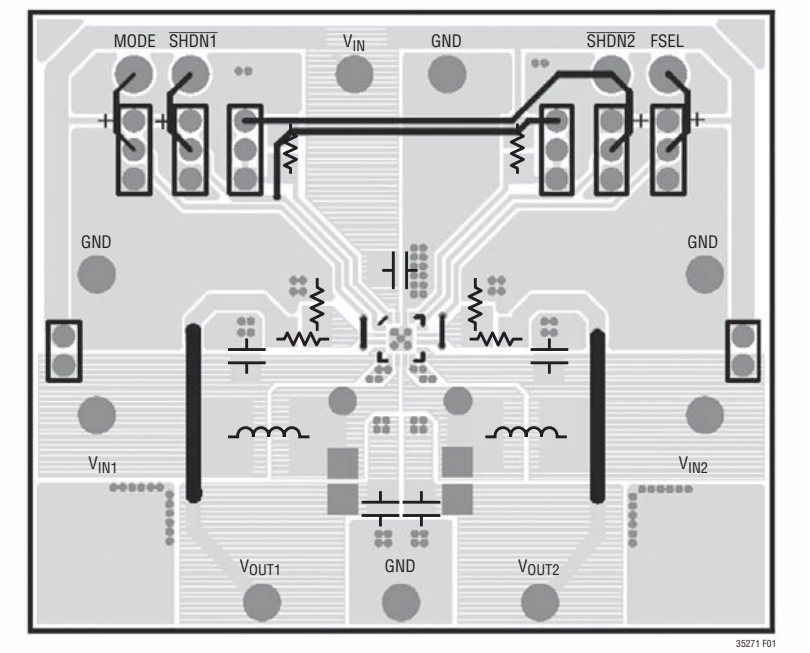


Figure 1. Recommended Component Placement for a Dual-Layer Board

APPLICATIONS INFORMATION

Table 1. Recommended Inductors

VENDOR	PART/STYLE	L (μH)	MAXIMUM CURRENT (mA)	DCR (Ω)	DIMENSIONS L × W × H (mm)
Coilcraft www.coilcraft.com	MSS5131 MSS4020 ME3220	2.2-10 3.3-10 1-10	1900-870 1100-540 3000-780	0.023-0.083 0.085-0.210 0.05-0.90	5.1 × 5.1 × 1 4 × 4 × 2 3.2 × 2.5 × 2
Coiltronics www.cooperet.com	SD10 SD12	1-10 1.2-10	1930-760 2450-818	0.045-0.289 0.037-0.284	5.2 × 5.2 × 1 5.2 × 5.2 × 1.2
FDK www.fdk.com	MIP3226D MIPF2520D	1.5-6.8 1.5-4.7	1400-1000 1500-1000	0.07-0.12 0.07-0.11	3.2 × 2.6 × 1 2.5 × 2 × 1
Murata www.murata.com	LQH43C LQH32C	1-10 1-4.7	1080-650 800-650	0.08-0.24 0.09-0.15	4.5 × 3.2 × 2.6 3.2 × 2.5 × 2
Sumida www.sumida.com	CDRH3D16 CDRH2D14	4.7-15 4.7-12	900-450 680-420	0.11-0.29 0.12-0.32	3.8 × 3.8 × 1.8 3.2 × 3.2 × 1.5
TDK www.global.tdk.co.jp	VLF3010A VLF5012A	1.5-10 2.2-10	1200-490 1500-800	0.068-0.58 0.090-0.30	2.6 × 2.8 × 1 4.5 × 4.7 × 1.2
Taiyo Yuden www.t-yuden.com	NR3010 NR3015	4.7-15 4.7-15	750-400 1000-560	0.19-0.74 0.12-0.36	3 × 3 × 1 3 × 3 × 1.5

Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 10μF output capacitor is sufficient for most applications. Larger values up to 22μF may be used to obtain lower output voltage ripple and improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used.

The internal loop compensation of the LTC3527/LTC3527-1 is designed to be stable with output capacitor values of 4.7μF or greater. Although ceramic capacitors are recommended, low ESR tantalum capacitors may be used as well.

A small ceramic capacitor in parallel with a larger tantalum capacitor may be used in demanding applications which have large load transients. Another method of improving the transient response is to add a small feedforward capacitor across the top resistor of the feedback divider [from V_{OUT1} (V_{OUT2}) to FB1 (FB2)]. A typical value of 15pF will generally suffice.

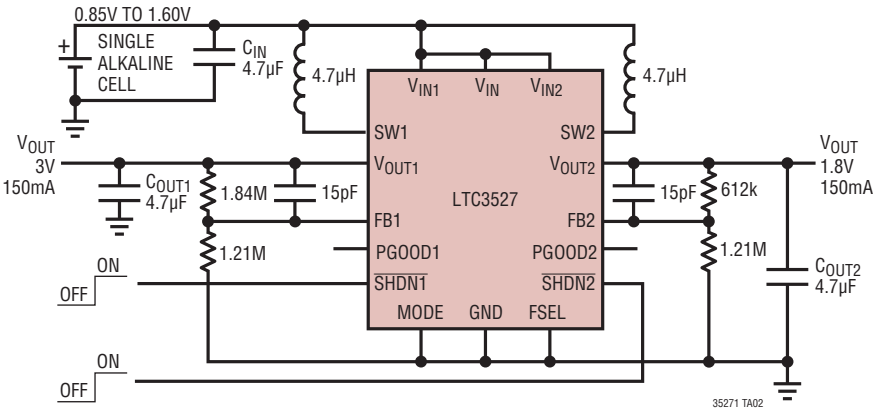
Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 2.2μF input capacitor is sufficient for most applications, although larger values may be used without limitations. Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their selection of ceramic parts.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	WEBSITE
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com
Taiyo-Yuden	(408) 573-4150	www.t-yuden.com
TDK	(847) 803-6100	www.component.tdk.com

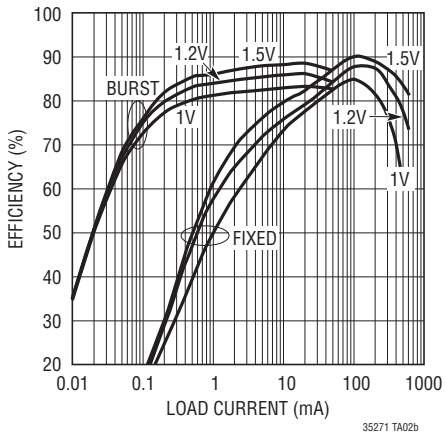
TYPICAL APPLICATIONS

1.2MHz, 1-Cell to V_{OUT1} = 3V, V_{OUT2} = 1.8V

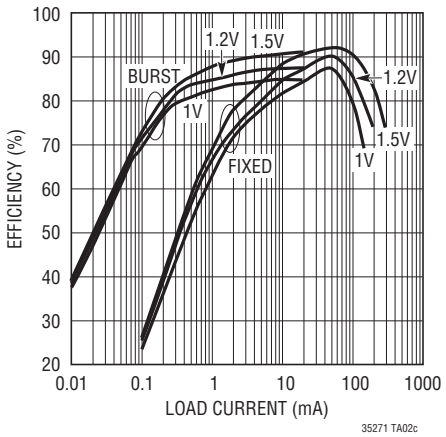


L: SUMIDA CDRH3D164R7
C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD

Boost 1 Efficiency

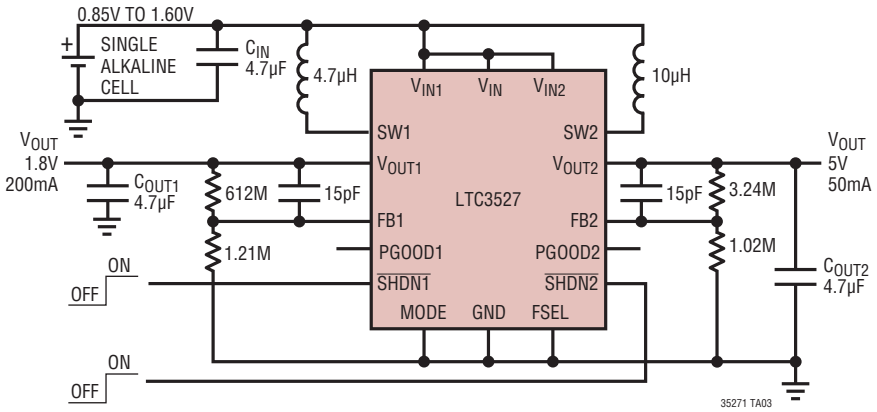


Boost 2 Efficiency



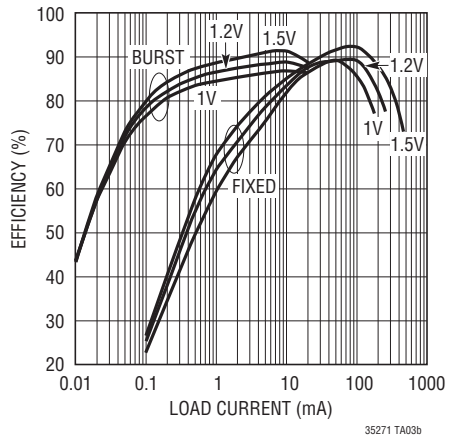
TYPICAL APPLICATIONS

1.2MHz, 1-Cell to V_{OUT1} = 1.8V, V_{OUT2} = 5V

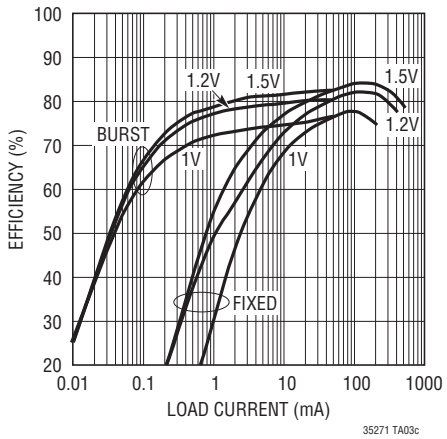


L: SUMIDA CDRH3D164R7
C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD

Boost 1 Efficiency

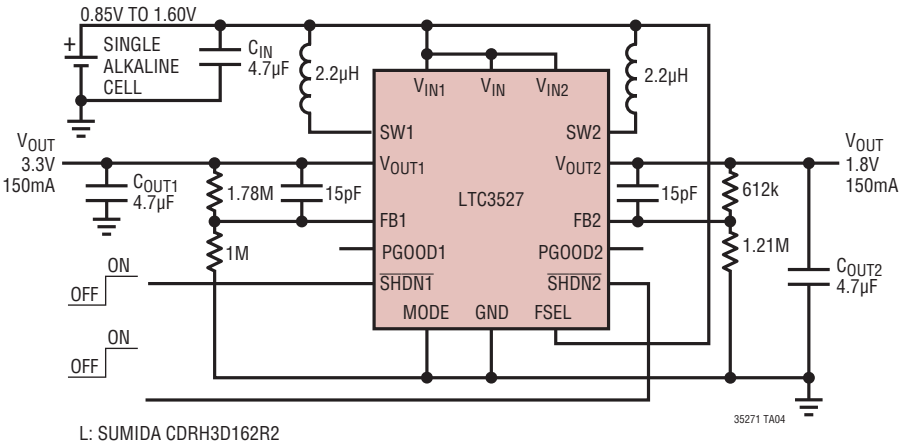


Boost 2 Efficiency



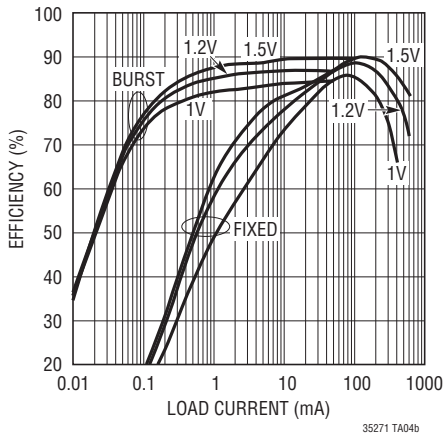
TYPICAL APPLICATIONS

2.2MHz, 1-Cell to V_{OUT1} = 3.3V, V_{OUT2} = 1.8V

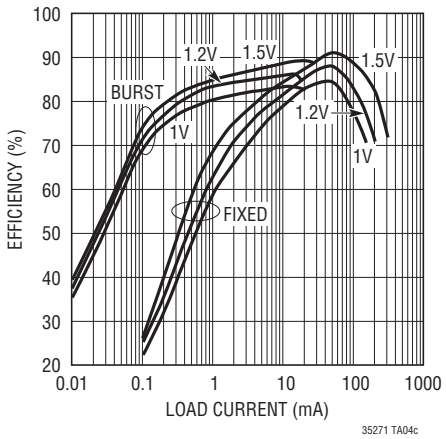


L: SUMIDA CDRH3D162R2
C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD

Boost 1 Efficiency

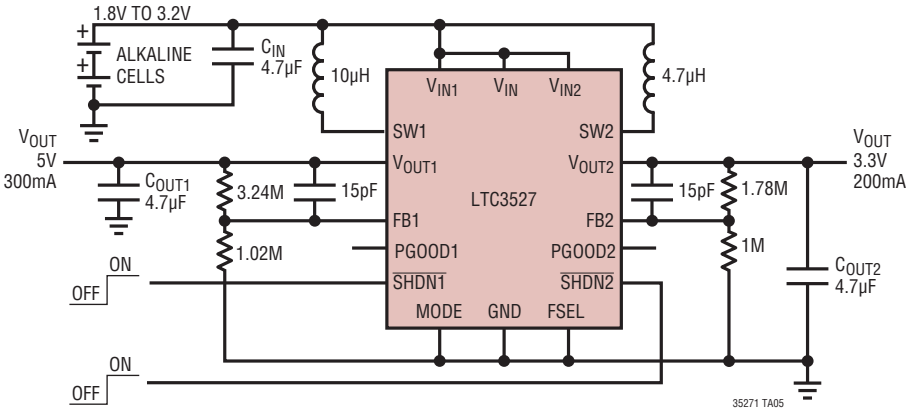


Boost 2 Efficiency



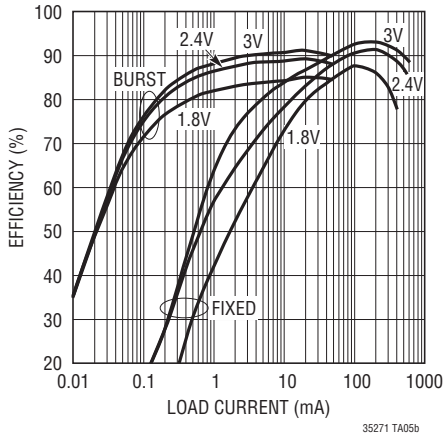
TYPICAL APPLICATIONS

1.2MHz, 2-Cell to V_{OUT1} = 5V, V_{OUT2} = 3.3V

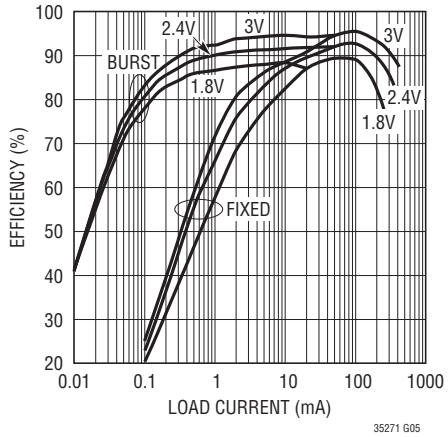


L: SUMIDA CDRH3D164R7
C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD

Boost 1 Efficiency

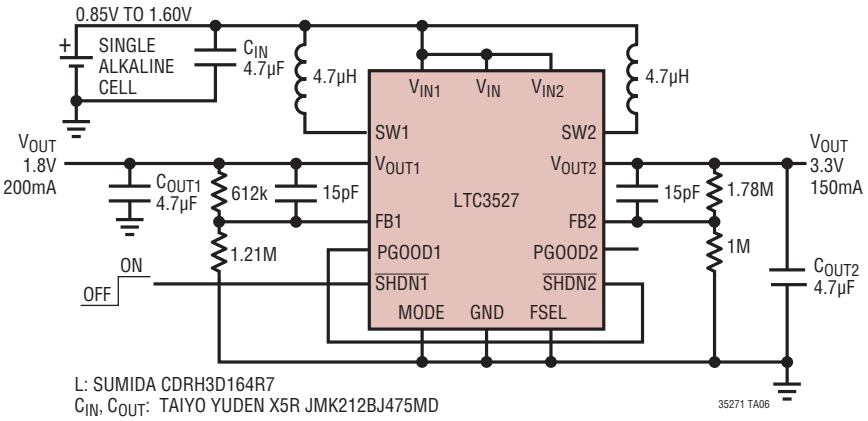


Boost 2 Efficiency



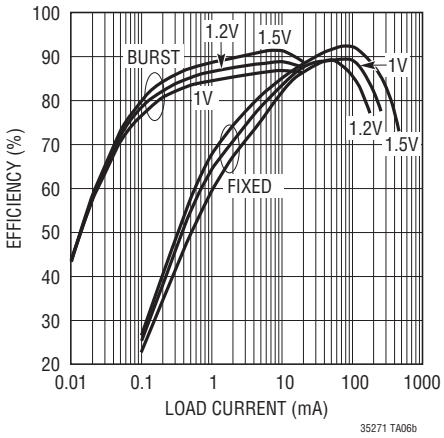
TYPICAL APPLICATIONS

Sequenced Start-Up V_{OUT1} to V_{OUT2}
1.2MHz, 1-Cell to V_{OUT1} = 1.8V, V_{OUT2} = 3.3V

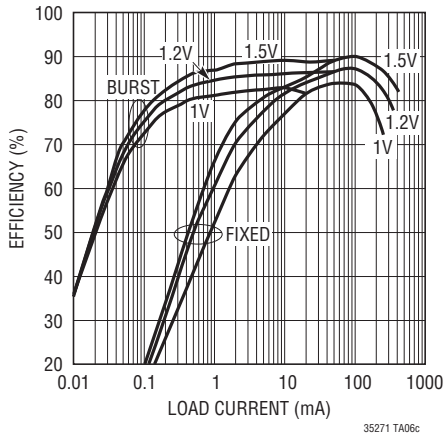


L: SUMIDA CDRH3D164R7
C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD

Boost 1 Efficiency

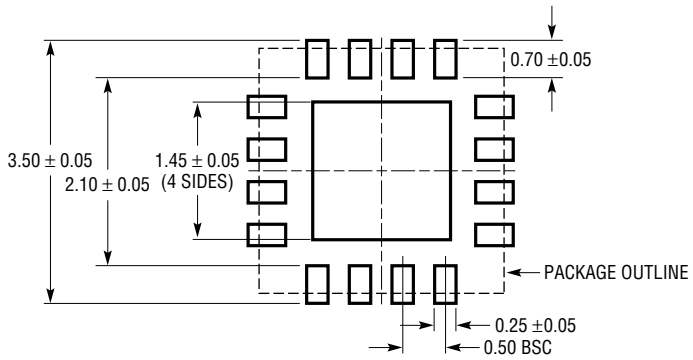


Boost 2 Efficiency

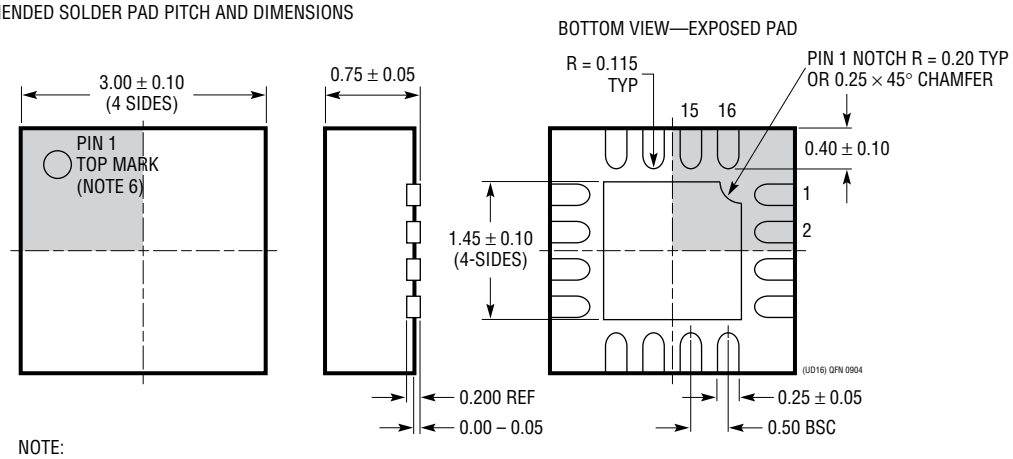


PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/09	Changes to Typical Applications	1, 15, 16, 17, 18, 19
		Change to Operation Section	12
		Changes to Applications Information Section	14

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3400/ LTC3400B	600mA I_{SW}, 1.2MHz Synchronous Step-Up DC/DC Converters	92% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$ = 5V, I_Q = 19µA/300µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3401	1A I_{SW}, 3MHz Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 6V, I_Q = 38µA, I_{SD} < 1µA, 10-Lead MS Package
LTC3421	3A I_{SW}, 3MHz Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN-24 Package
LTC3422	1.5A I_{SW}, 3MHz Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 25µA, I_{SD} < 1µA, 3mm × 3mm DFN Package
LTC3423/ LTC3424	2A I_{SW}, 3MHz Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 6V, I_Q = 38µA, I_{SD} < 1µA, 10-Lead MS Package
LTC3426	2A I_{SW}, 1.2MHz Synchronous Step-Up DC/DC Converter	92% Efficiency, V_{IN}: 1.6V to 4.3V, $V_{OUT(MAX)}$ = 5V, I_{SD} < 1µA, SOT-23 Package
LTC3428	500mA I_{SW}, 1.25MHz/2.5MHz Synchronous Step-Up DC/DC Converter with Output Disconnect	92% Efficiency, V_{IN}: 1.8V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_{SD} < 1µA, 2mm × 2mm DFN Package
LTC3429	600mA I_{SW}, 500kHz Synchronous Step-Up DC/DC Converter with Output Disconnect and Soft-Start	96% Efficiency, V_{IN}: 0.5V to 4.4V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA/300µA, I_{SD} < 1µA, ThinSOT Package
LTC3458	1.4A I_{SW}, 1.5MHz Synchronous Step-Up DC/DC Converter/ Output Disconnect/Burst Mode Operation	93% Efficiency, V_{IN}: 1.5V to 6V, $V_{OUT(MAX)}$ = 7.5V, I_Q = 15µA, I_{SD} < 1µA, DFN-12 Package
LTC3458L	1.7A I_{SW}, 1.5MHz Synchronous Step-Up DC/DC Converter with Output Disconnect, Automatic Burst Mode Operation	94% Efficiency, $V_{OUT(MAX)}$ = 6V, I_Q = 12µA, DFN-12 Package
LTC3459	70mA I_{SW}, 10V Micropower Synchronous Boost Converter/ Output Disconnect/Burst Mode Operation	V_{IN}: 1.5V to 5.5V, $V_{OUT(MAX)}$ = 10V, I_Q = 10µA, I_{SD} < 1µA, ThinSOT Package
LTC3525L-3	500mA I_{SW}, 1.2MHz Synchronous Step-Up DC/DC Converters with Output Disconnect, Automatic Burst Mode Operation	94% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 7µA, I_{SD} < 1µA, SC70 Package
LTC3526/ LTC3526B	500mA I_{SW}, 1.2MHz Synchronous Step-Up DC/DC Converters with Output Disconnect, Automatic Burst Mode Operation (LTC3526), PWM Only (LTC3526B)	94% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 10µA/300µA, I_{SD} < 1µA, 2mm × 2mm DFN Package
LTC3528/ LTC3528B	1A, 1MHz Synchronous Step-Up DC/DC Converter with Output Disconnect, Automatic Burst Mode Operation, PWM Only (LTC3528B)	94% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 10µA/300µA, I_{SD} < 1µA, 2mm × 3mm DFN Package

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