

# MC74ACT640

## Octal 3-State Inverting Transceiver

The MC74ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus  $\bar{A}$  to bus B when  $T/\bar{R} = \text{HIGH}$ , or from bus  $\bar{B}$  to bus A when  $T/\bar{R} = \text{LOW}$ . The enable input can be used to disable the device so the buses are effectively isolated.

### Features

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source -24 mA
- TTL Compatible Inputs
- Pb-Free Packages are Available\*

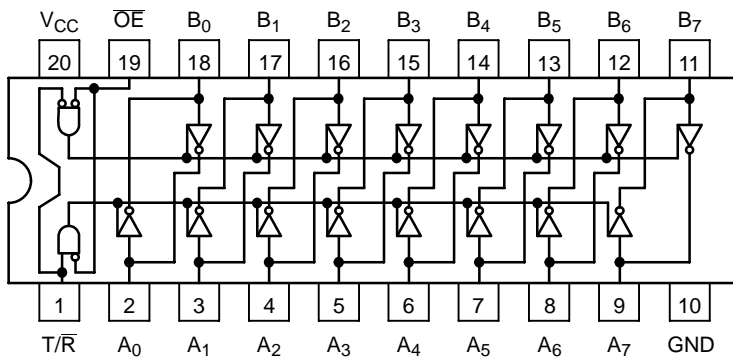


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

### PIN ASSIGNMENT

PIN	FUNCTION
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or 3-State Outputs

### TRUTH TABLE

OE	T/R	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	$\bar{A}$ to B	L
L	H	L	$\bar{A}$ to B	H
L	L	H	$\bar{B}$ to A	L
L	L	L	$\bar{B}$ to A	H

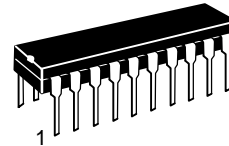
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

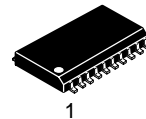


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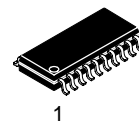
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PDIP-20  
N SUFFIX  
CASE 738



SOIC-20W  
DW SUFFIX  
CASE 751D



SOEIAJ-20  
M SUFFIX  
CASE 967

### ORDERING INFORMATION

Device	Package	Shipping†
MC74ACT640N	PDIP-20	18 Units/Rail
MC74ACT640NG	PDIP-20 (Pb-Free)	18 Units/Rail
MC74ACT640DW	SOIC-20	38 Units/Rail
MC74ACT640DWG	SOIC-20 (Pb-Free)	38 Units/Rail
MC74ACT640DWR2	SOIC-20	1000 / Tape & Reel
MC74ACT640DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74ACT640MEL	SOEIAJ-20	2000 / Tape & Reel
MC74ACT640MELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V	
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V	
$V_O$	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V	
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA	
$I_{OK}$	DC Output Diode Current	$\pm 50$	mA	
$I_O$	DC Output Sink/Source Current	$\pm 50$	mA	
$I_{CC}$	DC Supply Current per Output Pin	$\pm 50$	mA	
$I_{GND}$	DC Ground Current per Output Pin	$\pm 50$	mA	
$T_{STG}$	Storage Temperature Range	-65 to +150	°C	
$T_L$	Lead temperature, 1 mm from Case for 10 Seconds	260	°C	
$T_J$	Junction temperature under Bias	+150	°C	
$\theta_{JA}$	Thermal resistance	PDIP SOIC	67 96	°C/W
$P_D$	Power Dissipation in Still Air at 85°C	PDIP SOIC	750 500	mW
MSL	Moisture Sensitivity	Level 1		
$F_R$	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 > 1000	V
$I_{Latchup}$	Latchup Performance	Above $V_{CC}$ and Below GND at 85°C (Note 5)	$\pm 100$	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	DC Input Voltage (Referenced to GND)	4.5		5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0		$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	25	+85	°C
$t_r, t_f$	Input Rise and Fall Time (Note 7)	$V_{CC} = 4.5\text{ V}$ $V_{CC} = 5.5\text{ V}$	0 10 8.0	10 10 8.0	ns/V
$T_J$	Junction Temperature (PDIP)			140	°C
$I_{OH}$	Output Current – High			-24	mA
$I_{OL}$	Output Current – Low			24	mA

6. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
7.  $V_{in}$  from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

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## DC CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
		5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V
		5.5	1.5	0.8	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5		3.86	3.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -24 mA I <sub>OH</sub> -24 mA
		5.5		4.86	4.76		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1		
I <sub>IN</sub>	Maximum Input Leakage Current	4.5		0.36	0.44	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -24 mA I <sub>OH</sub> -24 mA
		5.5		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
ΔI <sub>CCT</sub>	Additional Max. I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V
I <sub>OZ</sub>	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>OLD</sub> I <sub>OHD</sub>	†Minimum Dynamic Output Current	5.5 5.5			75 -75	mA mA	V <sub>OLD</sub> = 1.65 V Max
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS t<sub>r</sub> = t<sub>f</sub> = 3.0 ns (For Figures and Waveforms, See Figures 2 and 3.)

Symbol	Parameter	V <sub>CC</sub> * (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay An to Bn or Bn to An	5.0	1.5	8.0	1.0	8.5	ns
t <sub>PHL</sub>	Propagation Delay An to Bn or Bn to An	5.0	1.5	8.0	1.0	9.0	ns
t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t <sub>PHZ</sub>	Output Disable Time T/ $\overline{R}$ or $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t <sub>PLZ</sub>	Output Disable Time T/ $\overline{R}$ or $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns

\*Voltage Range 5.0 V is 5.0 V ±0.5 V

## CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>I/O</sub>	Input/Output Capacitance	15	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	45	pF	V <sub>CC</sub> = 5.0 V

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## SWITCHING WAVEFORMS

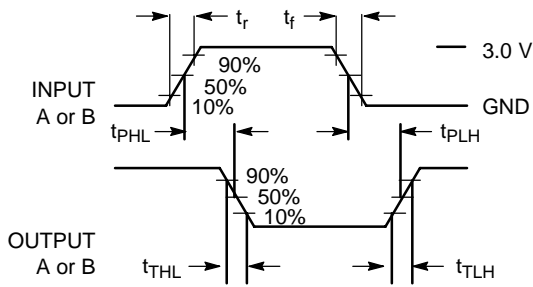


Figure 2.

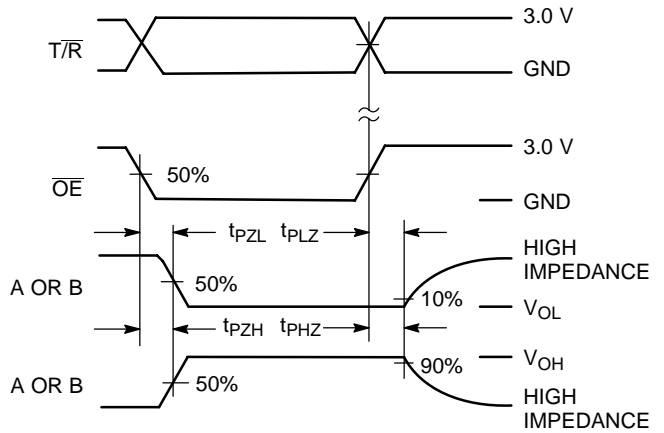
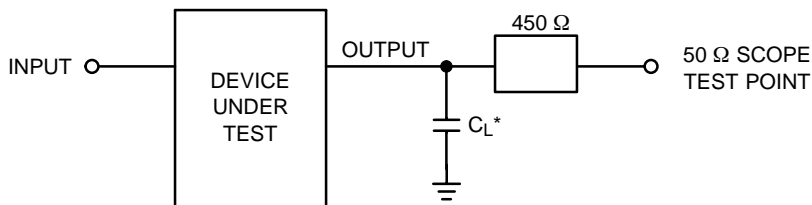


Figure 3.

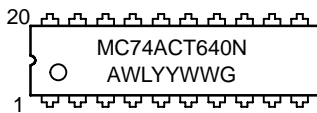


\*Includes all probe and jig capacitance

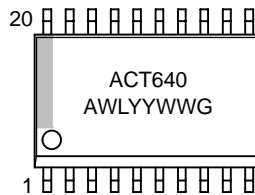
Figure 4. Test Circuit

## MARKING DIAGRAMS

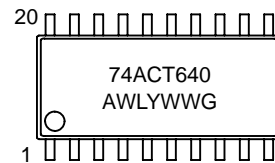
### PDIP-20



### SOIC-20W



### SOEIAJ-20

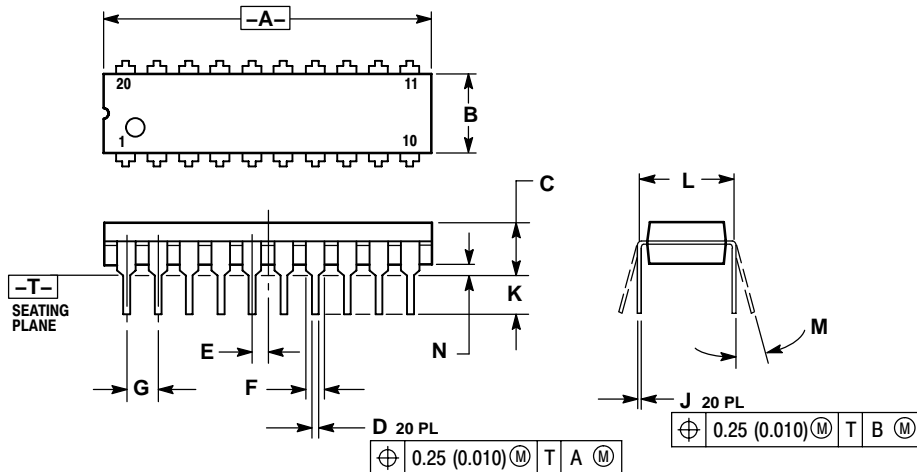


A = Assembly Location  
 WL = Wafer Lot  
 YY, Y = Year  
 WW = Work Week  
 G = Pb-Free Package

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## PACKAGE DIMENSIONS

PDIP-20  
N SUFFIX  
PLASTIC DIP PACKAGE  
CASE 738-03  
ISSUE E

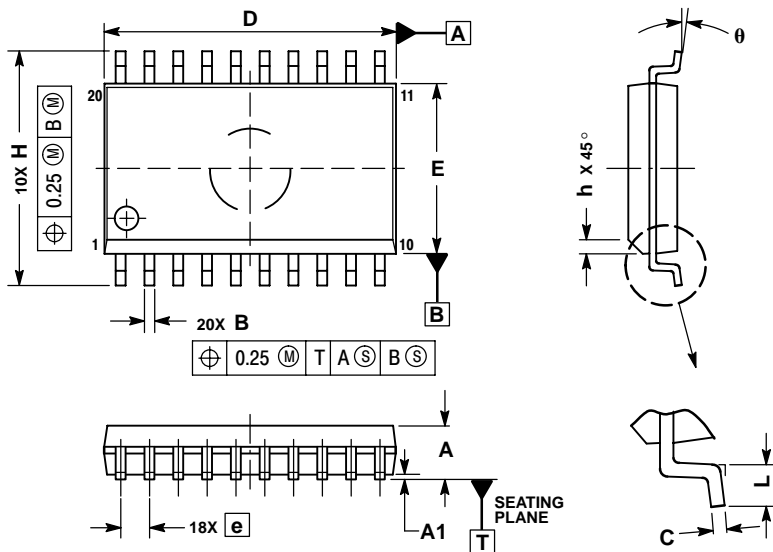


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOIC-20W  
DW SUFFIX  
CASE 751D-05  
ISSUE G



NOTES:

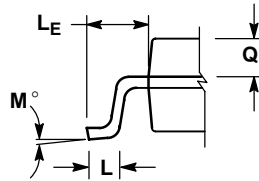
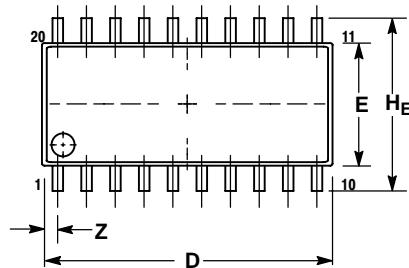
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

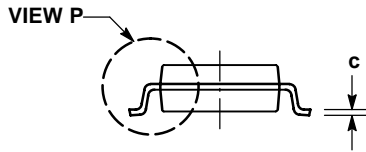
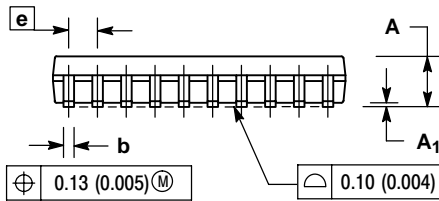
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## PACKAGE DIMENSIONS

SOEIAJ-20  
M SUFFIX  
CASE 967-01  
ISSUE A



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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