TMD3700

Color, ALS and Proximity Sensor Module

General Description

The device features advanced Proximity measurement, Digital Ambient Light Sensing (ALS) and Color Sensing (CRGB). The slim module incorporates an IR LED and factory calibrated LED driver. The Proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED).

Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings.

The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The Color and ALS detection feature provides red, green, blue and clear light intensity data. Each of the C, R, G, B channels have a UV and IR blocking filters and a dedicated data converter producing16-bit data simultaneously. This architecture allows applications to accurately measure ambient light and sense color which enables devices to calculate illuminance and color temperature, control display backlight, and chromaticity.

Ordering Information and Content Guide appear at end of datasheet.

Figure 1:
Added Value of Using TMD3700

Benefits	Features
• Reduced board space requirements and enables low-profile system design	• Small footprint and low profile package 4.00 x 1.75 x 1.00 mm
• Improved ALS angular response for more accurate measurement of lighting environment	• 45 degree average ALS FOV
• Operating range of 200 milli-Lux to 60 kilo-Lux enables operation behind dark glass	• Wide dynamic range and high sensitivity

Benefits	Features
• Single device integrated optical solution	• RGB, Ambient Light Sensor (ALS) and proximity support • Power management features • I²C fast mode interface compatible • Integral IR LED
• Accurate color temperature and ambient light sensing	• UV / IR blocking filters • Programmable gain and integration time
• Reduced power consumption	• 0.18µ process technology with 1.8V I²C bus

Applications

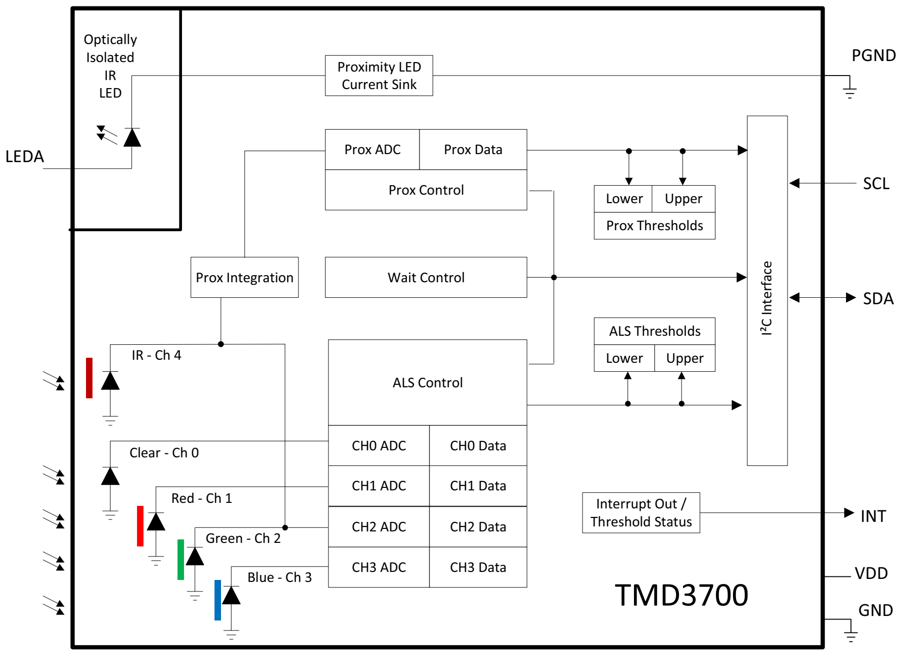
The TMD3700 applications include:

- Color Sensing
- Ambient Light Sensing
- Mobile Phone touch screen disable

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD3700



Pin Assignment

Top View of module showing pin assignment

Figure 3:
TMD3700 Pinout (Top View)

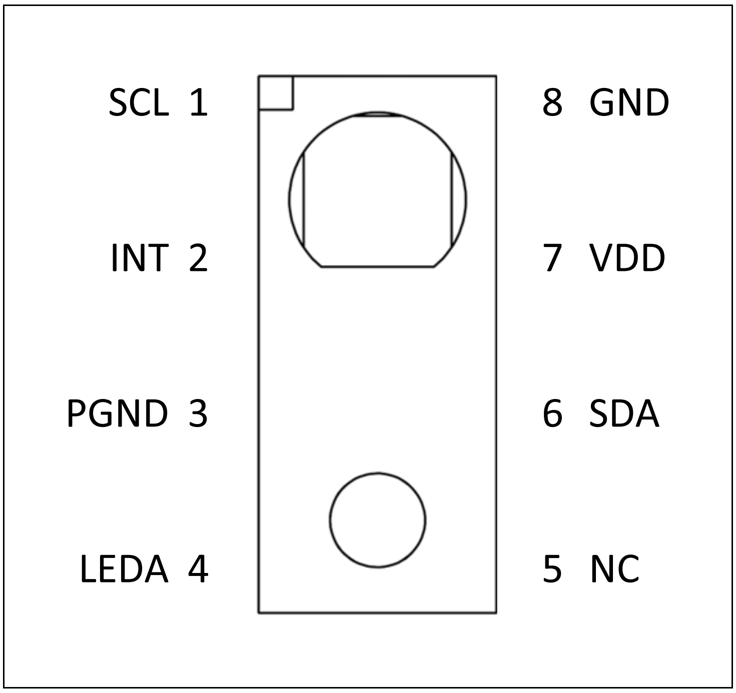


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	SCL	I^2C serial clock input terminal
2	INT	Interrupt. Open drain output (active low).
3	PGND	Ground for LED current sink.
4	LEDA	LED anode
5	NC	No connection
6	SDA	I^2C serial data I/O terminal
7	VDD	Supply voltage
8	GND	Ground. All voltages are referenced to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD	Supply voltage	-0.3	2.2	V
LEDA	Supply voltage	-0.3	3.6	V
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V
(SDA, INT)	Output terminal current	-1	20	mA
T_{Strg}	Storage temperature range	-40	85	ºC
I_{SCR}	Input current (latch up immunity) JEDEC JESD78D Nov 2011	CLASS 1		
ESD_{HBM}	Electrostatic discharge HBM S-001-2014	±2000		V
ESD_{CDM}	Electrostatic discharge CDM JEDEC JESD22-C101F Oct 2013	±500		V

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
V_{LEDA}	Voltage supplied to LEDA pin	3.0 (2)	3.3	3.6	V
T_A	Operating free-air temperature (1)	-30		85	°C

Note(s):
1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.
2. Minimum VLED for pldrive of 100mA or less.

Figure 7:
Operating Characteristics, V_{DD} = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.0		MHz
IDD	Supply current (1)	Active ALS state (PON=AEN=1, PEN= 0) (2)	20	90	150	µA
		Idle state (PON=1, AEN=PEN=0) (3)		30	60	
		Sleep state (4)		0.7	5.0	µA
VOL	INT, SDA output low voltage	6 mA sink current			0.6	V
ILEAK	Leakage current, SDA, SCL, INT, pins	Leakage current at 0V = ± 50nA Leakage current at 3V = ± 50nA	-50		50	nA
VIH	SCL, SDA input high voltage		1.26			V
VIL	SCL, SDA input low voltage				0.54	V
T_{ACTIVE}	Time from power-on to ready to receive I²C commands			1.5		ms

Note(s):
1. Values are shown at the VDD pin and do not include current through the IR LED.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Figure 8:
Optical Characteristics

Parameter	Test Conditions	Clear Channel			Units
		Min	Typ	Max	
Re Irradiance responsivity settings: AGAIN = 16x ATIME = 400mS	λ_D = 465 nm LED, 53.8 μW/cm^2		112		count/(μW/cm^2)
	λ_D = 530 nm LED, 43.9 μW/cm^2		152		
	λ_D = 620 nm LED, 37.5 μW/cm^2		193		
	Warm white LED, 45.6 μW/cm^2		152		
	Warm white LED, 45.6 μW/cm^2	5950	7000	8050	counts
		IR Channel			
		Min	Typ	Max	
	λ_D = 950 nm LED, 21.1 μW/cm^2		137		count/(μW/cm^2)

Figure 9:
ALS Operating Characteristics, VDD = 1.8 V, T_A = 25°C, AGAIN = 16x, ATIME = 0xF6 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size		2.68	2.78	2.90	ms
Dark ADC count value	Ee = 0 μW/ cm^2 AGAIN: 64x ATIME: 100ms (0xDC)	0	1	3	counts
Gain scaling, relative to 1x gain setting	AGAIN: 4x		4		x
	AGAIN: 16x		16		
	AGAIN: 64x		64		
ADC noise	AGAIN: 16x		0.005		% full scale
Lux accuracy (1)	White LED, 2700K	90	100	110	%

Note(s):

1. Not production tested. Representative result by laboratory characterization.

Figure 10:
Proximity Operating Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Part to part variation[1]	Conditions: PGAIN = 2 (4x) PLDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance	75	100	125	%
Response, absolute	Basic proximity measurement Conditions: PGAIN = 2 (4x) PLDRIVE = 16 (102mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 2 (16µs) Target material: 90% reflective surface of Kodak gray card Target Size: 100mm x 100mm Target Distance: 100mm Module held by TMD37003SH210T socket	90	113	136	counts
	Improved accuracy proximity measurement using factory programmed offsets in each device and a supplied driver	85	100	115	
Response, no target using offset values from 0xE6 and 0xE7	PGAIN = 2 (4x) ILEDDRIVE = 16 (102mA) PPULSE = 16 (17 Pulses) Pulse Length = 2 (16µs)	0		12	counts
Noise/Signal[3]	PGAIN = 2 (4x) IRLEDDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance			1	%

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization.
3. Production tested result is the average of 20 readings divided by the average response.

Figure 11:
Spectral Response

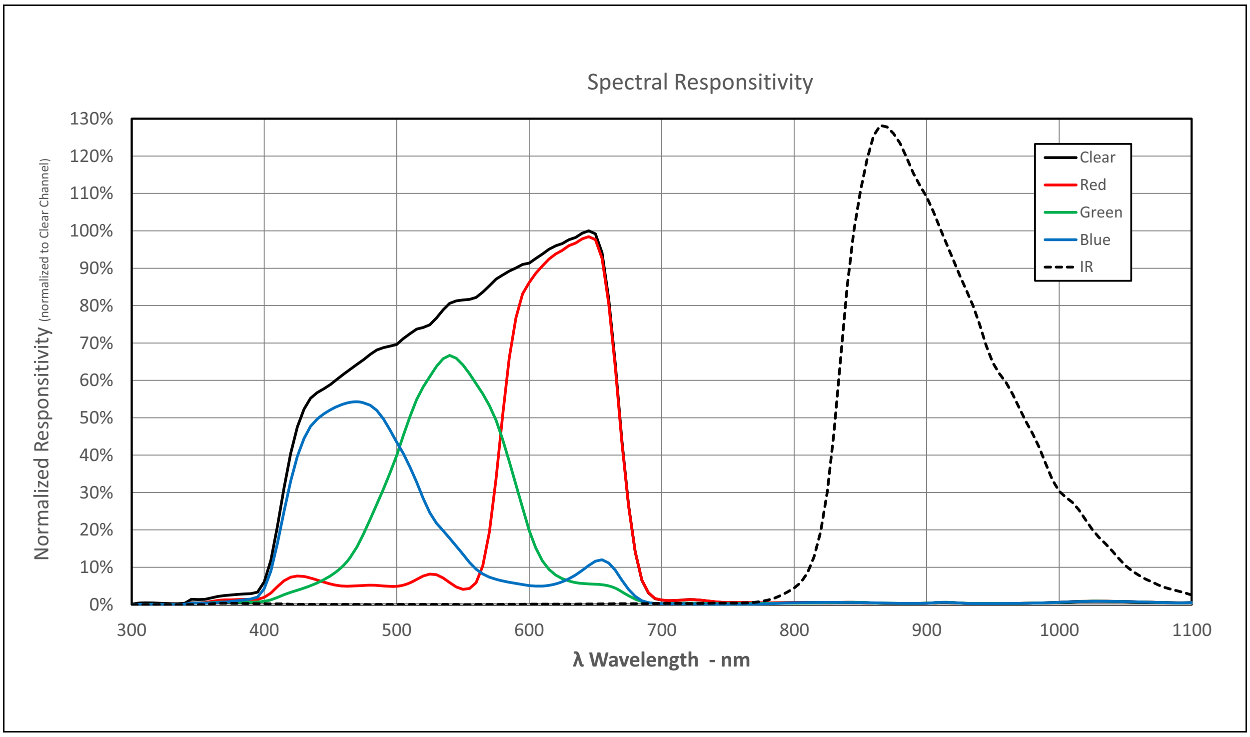


Figure 12:
ALS Average Angular Response

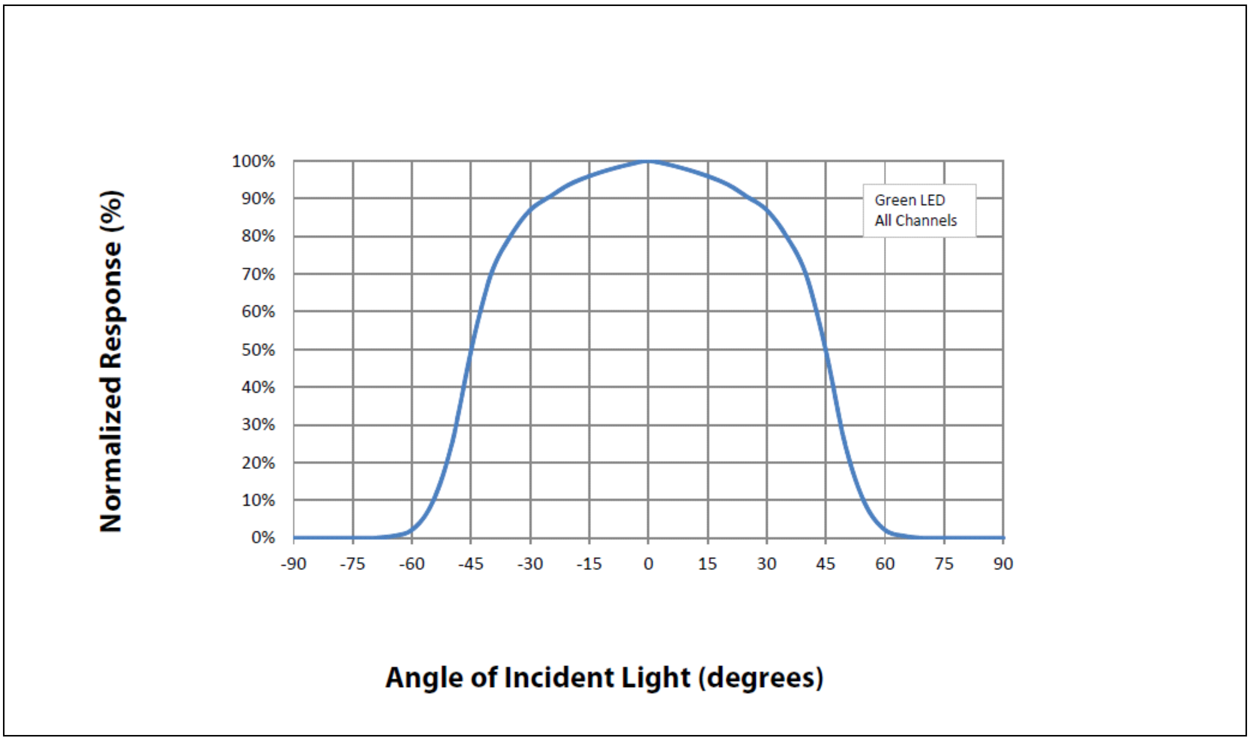


Figure 13:
CRGB Optical Characteristics

Parameter	Test Conditions	Red / Clear Channel		Green / Clear Channel		Blue / Clear Channel	
		Min	Max	Min	Max	Min	Max
Color ADC count value ratio: color / clear	λ_D = 465 nm	0%	20%	0%	55% (1)	80%	100%
	λ_D = 525 nm	0%	30% (1)	65%	90%	0%	50% (1)
	λ_D = 615 nm	80%	110%	0%	20%	0%	20%
	White LED, 2700 k	50%	70%	24%	45%	10%	35%

Note(s):

1. Not production tested.

Figure 14:
Illuminance (Lux) vs Counts (Clear Channel)

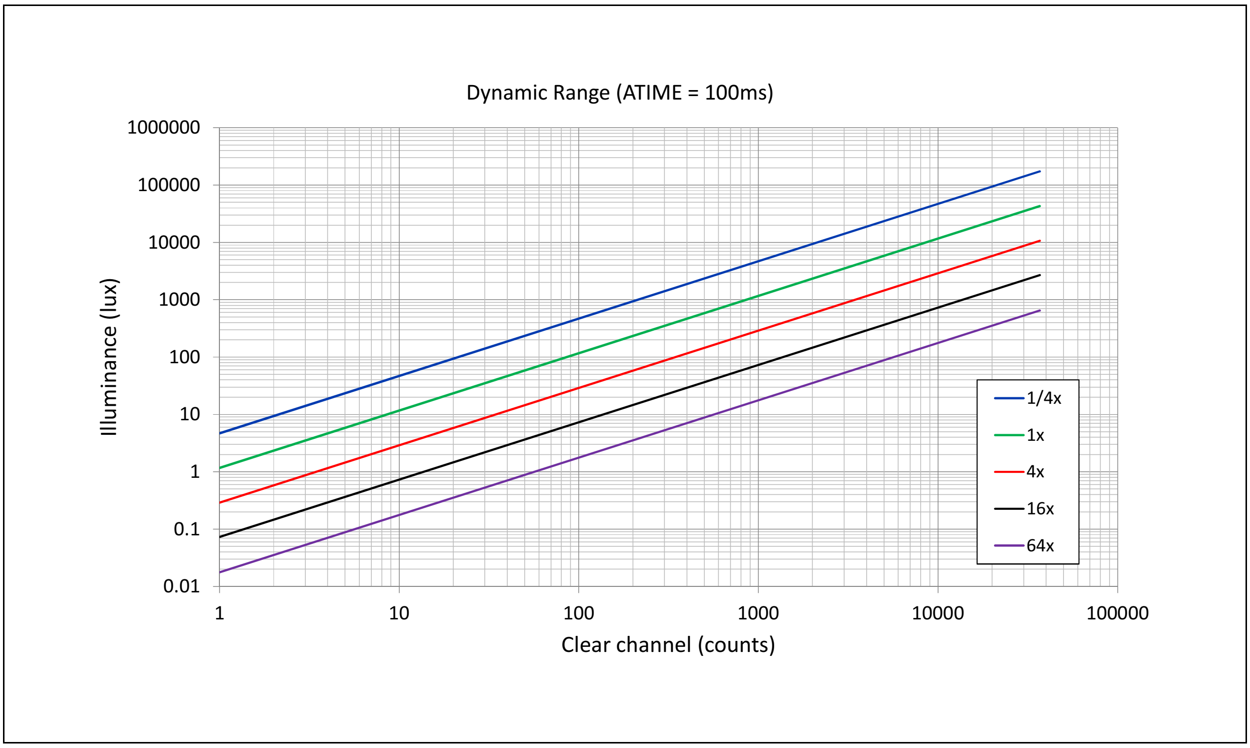
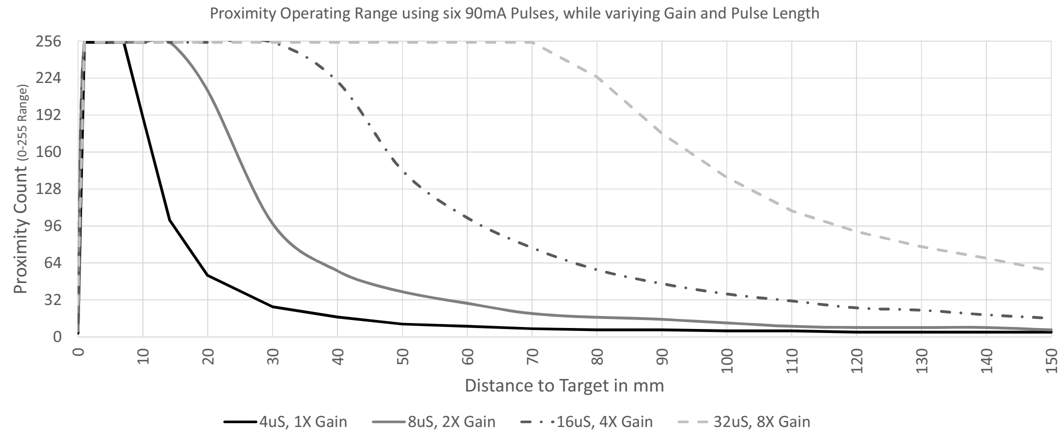
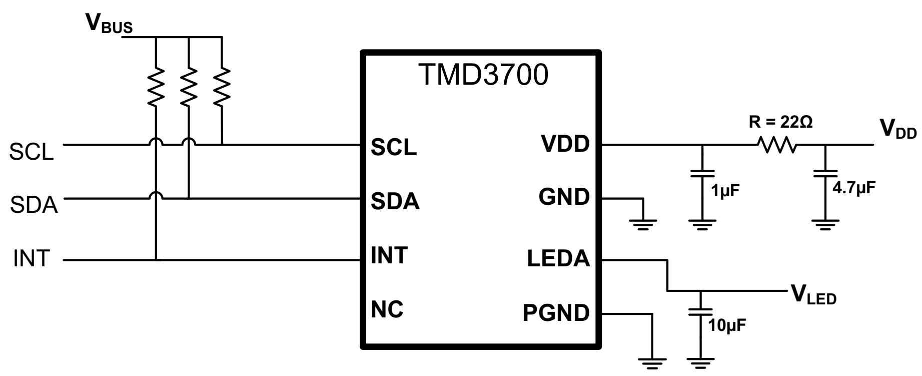


Figure 15:
Proximity Operation



By varying Gain, LED drive current, number of LED pulses and LED pulse duration the proximity detection range can be adjusted.

Figure 16:
Proximity Test Circuit



Note(s):

1. Place the 1µF and 10µF capacitors as close as possible to the module.
2. V_{DD} = 1.8V, V_{BUS} = 1.8V, V_{LED} = 3.3V.

I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Register Description

Figure 17:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ADC integration time	0x00
0x82	PRATE	R/W	Proximity sample rate	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILT	R/W	Proximity interrupt low threshold	0x00
0x8A	PIHT	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	ALS and proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Wait Long	0x80
0x8E	PCFG0	R/W	Proximity pulse width and count	0x80
0x8F	PCFG1	R/W	Proximity gain and LED current	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	
0x92	ID	R	Device ID	0xC0
0x93	STATUS	R, SC	Device status register one	0x00
0x94	CDATAL	R	Clear ADC low data register	0x00
0x95	CDATAH	R	Clear ADC high data register	0x00
0x96	RDATAL	R	Red ADC low data register	0x00
0x97	RDATAH	R	Red ADC high data register	0x00
0x98	GDATAL	R	Green ADC low data register	0x00
0x99	GDATAH	R	Green ADC high data register	0x00
0x9A	BDATAL	R	Blue ADC low data register	0x00
0x9B	BDATAH	R	Blue ADC high data register	0x00
0x9C	PDATA	R	Proximity ADC data register MSBs	0x00
0x9F	CFG2	R/W	LSB of ALS gain	0x04

Address	Register Name	R/W	Register Function	Reset Value
0xAB	CFG3	R/W	Configuration register three	0x00
0xC0	POFFSET_L	R/W	Proximity offset magnitude	0x00-0xFF
0xC1	POFFSET_H	R/W	Proximity offset sign	0x00-0xFF
0xD7	CALIB	R/W	Calibration control	0x00
0xD9	CALIBCFG	R/W	Calibration configuration	0x00
0xDC	CALIBSTAT	R/W	Calibration status bit	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00

Note(s):

- R = Read Only
- W = Write Only
- R/W = Read or Write
- SC = Self Clearing after access

ENABLE Register (0x80)

Figure 18:
ENABLE Register

0x80: ENABLE				
Field	**Name**	**Reset**	**Type**	**Description**
7:4	Reserved	0	RW	Reserved.
3	wen	0	RW	Wait Enable. This bit activates the wait feature. Writing a one actives the wait timer. Writing a zero disables the wait timer.
2	pen	0	RW	Proximity Detect Enable. This field activates the proximity detection.
1	aen	0	RW	ALS Enable. This bit actives the ALS function. Set aen=1 and pon=1 in the same command to ensure autozero function is run prior to the first measurement.
0	pon	0	RW	Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator.

The Mode/Parameter fields should be written before aen or pen is asserted. The functions pen and aen require pon to be asserted for the respective function to operate correctly.

ATIME Register (0x81)

Figure 19:
ATIME Register

<table>
<tr><th colspan="8">0x81: ATIME</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="4">Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">atime</td><td rowspan="8">0x00</td><td rowspan="8">RW</td><td colspan="4">Integration Time. Eight bit value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms, 0x01 indicates 5.6ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.</td></tr>
<tr><th>Value</th><th>Integration Cycles</th><th>Integration Time</th><th>Maximum ALS Value</th></tr>
<tr><td>0x00</td><td>1</td><td>2.8ms</td><td>1023</td></tr>
<tr><td>0x01</td><td>2</td><td>5.6ms</td><td>2047</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0x3f</td><td>63</td><td>180ms</td><td>65535</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>0xff</td><td>255</td><td>721ms</td><td>65535</td></tr>
</table>

The ATIME register controls the integration time of the ALS ADCs.

The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth.

Note(s): The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles: 125ns*11*8*256=2.81ms.

PRATE Register (0x82)

Figure 20:
PRATE Register

0x82: PRATE				
Field	Name	Reset	Type	Description
7:0	PRATE	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PRATE + 1)*88µs

WTIME Register (0x83)

Figure 21:
WTIME Register

0x83: WTIME						
Field	Name	Reset	Type	Description		
7:0	wtime	0x00	RW	ALS Wait Time. Eight bit value that specifies the time in 2.81ms to wait between ALS cycles.		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.8ms/ 33.8ms
				0x01	2	5.6ms/ 67.6ms
				...	...	...
				0x3f	63	180ms/ 2.16s
				...	...	...
				0xff	255	721ms/ 8.65s

The wait timer is implemented with a down counter with 0x00 as the terminal count. Loading 0x00 will generate a 2.81ms wait time, loading 0x01 will generate a 5.6ms wait time, and so forth; by asserting wlong, in register 0x8D the wait time is given in multiples of 33.8ms (12x).

AILTL Register (0x84)

Figure 22:
AILTL Register

0x84: AILTL				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	AILTL	0x00	RW	Low Byte of the Low Threshold

This register provides the low byte of the low interrupt ALS (C channel) threshold.

AILTH Register (0x85)

Figure 23:
AILTH Register

0x85: AILTH				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	AILTH	0x00	RW	High Byte of the Low Threshold

This register provides the high byte of the low interrupt ALS (C channel) threshold.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold. If the value generated by the C channel is below the low threshold specified and the APERS value is reached, the aint bit is asserted which will assert the INT pin if aien is set.

There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied then at the same time to avoid an invalid threshold (e.g. when going from 0x00ff to 0x0100, the invalid intermediate value 0x0000 is suppressed. This implies that 1) the LSB cannot be changed without writing to the MSB and 2) that writing to the LSB of one 16-bit value and afterwards to the MSB of another 16-bit register will write all 16 bits to the MSB related register.

AIHTL Register (0x86)

Figure 24:
AIHTL Register

0x86: AIHTL				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	AIHTL	0	RW	Low Byte of the High Threshold

This register provides the low byte of the high interrupt threshold.

AIHTH Register (0x87)

Figure 25:
AIHTH Register

0x87: AIHTH				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	AIHTH	0	RW	High Byte of the High Threshold

This register provides the low byte of the high interrupt threshold.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold. If the value generated by the C channel is above the high threshold specified and the APERS value is reached, the aint bit is asserted which will assert the INT pin if aien is set.

PILT Register (0x88)

Figure 26:
PILT Register

0x88: PILT				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	pilt	0	RW	Proximity ADC Channel Low Threshold

This register provides the low interrupt threshold.
If the value generated by the proximity channel is below the low threshold specified and the PPERS value is reached, the pint bit is asserted which will assert the INT pin if pien is set.

PIHT Register (0x8A)

Figure 27:
PIHT Register

0x8A: PIHT				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	piht	0	RW	Proximity ADC Channel High Threshold

This register provides the high interrupt threshold.
If the value generated by the proximity channel is above the high threshold specified and the PPERS value is reached, the pint bit is asserted which will assert the INT pin if pien is set.

PERS Register (0x8C)

Figure 28:
PERS Register

0x8C: PERS					
Field	**Name**	**Reset**	**Type**	**Description**	
7:4	ppers	0	RW	Proximity Persistence Filtering.	
				Value	**Interrupt generated when...**
				0	Every proximity cycle
				1	Any proximity value outside of threshold range
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				...	...
				15	15 consecutive proximity values out of range
3:0	apers	0	RW	**Value**	**Interrupt generated when...**
				0	Every ALS cycle
				1	Any ALS value outside of threshold range
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5...
				5	10...
				6	15...
				7	20...
				12	45...
				13	50...
				14	55...
				15	60 consecutive ALS values out of range

CFG0 Register (0x8D)

Figure 29:
CFG0 Register

0x8D: CFG0				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	Reserved	1 0 0 0 0	RW	Reserved. Must be set to 10000.
2	wlong	0	RW	Wait Long. When asserted, the wait cycle is increased by a factor 12x from that programmed in the WTIME register.
1:0	Reserved	0 0	RW	Reserved. Must be set to 00.

This register controls the interrupt filtering capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after either a proximity or ALS integration cycle or if the integration cycle has produced a result that is outside of the values specified by threshold register for some specified number of times. Separate filtering is provided for proximity and ALS functions.

ALS interrupts are generated by looking only at the ADC integration results of the C channel photodiode.

PCFG0 Register (0x8E)

Figure 30:
PCFG0 Register

<table>
<tr><th colspan="6">0x8E: PCFG0</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">ppulse_len</td><td rowspan="6">1</td><td rowspan="6">RW</td><td colspan="2">Proximity Pulse Length.</td></tr>
<tr><td>Value</td><td>Pulse Length</td></tr>
<tr><td>0</td><td>4μs</td></tr>
<tr><td>1</td><td>8μs</td></tr>
<tr><td>2</td><td>16μs</td></tr>
<tr><td>3</td><td>32μs</td></tr>
</table>

<table>
<tr><th colspan="6">0x8E: PCFG0</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="7">5:0</td><td rowspan="7">ppulse</td><td rowspan="7">15</td><td rowspan="7">RW</td><td colspan="2">Maximum Number of Pulses in Proximity.</td></tr>
<tr><td>Value</td><td>Number of Pulses</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>63</td><td>64</td></tr>
</table>

PCFG1 Register (0x8F)

Figure 31:
PCFG1 Register

<table>
<tr><th colspan="6">0x8F: PCFG1</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">pgain</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">Proximity Gain Control. Sets the gain of the proximity receiver.</td></tr>
<tr><td>Value</td><td>Gain Value</td></tr>
<tr><td>0</td><td>1x</td></tr>
<tr><td>1</td><td>2x</td></tr>
<tr><td>2</td><td>4x</td></tr>
<tr><td>3</td><td>8x</td></tr>
<tr><td>5</td><td>Reserved</td><td>0</td><td>RW</td><td colspan="2">Reserved.</td></tr>
<tr><td rowspan="6">4:0</td><td rowspan="6">pldrive</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="2">Proximity LED Drive Strength. This is configured linearly in steps of 6mA This is the nominal value. The actual value depends on the trim procedure.</td></tr>
<tr><td>Value</td><td>LED Current</td></tr>
<tr><td>0</td><td>6mA</td></tr>
<tr><td>1</td><td>12mA</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>31</td><td>192mA</td></tr>
</table>

CFG1 Register (0x90)

Figure 32:
CFG1 Register

0x90: CFG1				
Field	**Name**	**Reset**	**Type**	**Description**
7:2	Reserved	0	RW	Reserved.
1:0	again	0	RW	ALS Gain Control. Sets the gain of the ALS DAC. **Field Value** / **Gain**: 00 = 1x 01 = 4x 10 = 16x 11 = 64x

CFG1 Register: Register CFG1 sets the gain level for ALS measurements. The valid range of values is 0x00 - 0x03.

REVID Register (0x91)

Figure 33:
REVID Register

0x91: REVID				
Field	**Name**	**Reset**	**Type**	**Description**
7:4	Reserved	0000	R	Reserved.
3	Reserved	0	R	Reserved.
2:0	rev_id	010	R	Revision Number Identification

ID Register (0x92)

Figure 34:
ID Register

<table>
<tr><th colspan="6">0x92: ID</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">7:2</td><td rowspan="3">ID</td><td rowspan="3">110000</td><td rowspan="3">R</td><td colspan="2">Part Number Identification.</td></tr>
<tr><td>Value</td><td>Meaning</td></tr>
<tr><td>110000</td><td></td></tr>
<tr><td>1:0</td><td>Reserved</td><td></td><td></td><td colspan="2">Reserved.</td></tr>
</table>

STATUS Register (0x93)

Figure 35:
STATUS Register

0x93: STATUS				
Field	**Name**	**Reset**	**Type**	**Description**
7	asat	0	R, SC	ALS Saturation. This flag is set for analog saturation writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1
6	psat	0	R, SC	Proximity Saturation. Indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1
5	pint	0	R, SC	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt. writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1
4	aint	0	R, SC	ALSIntr. Indicates that the device is asserting an ALS interrupt. writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1
3	cint	0	R, SC	Calibration Interrupt. writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1
1	psat_ reflective	0	R, SC	psat interrupt is from reflective light saturation writing a 1 to psat or psat_reflective will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1

0x93: STATUS				
Field	**Name**	**Reset**	**Type**	**Description**
0	psat_ ambient	0	R, SC	psat interrupt is from ambient light or idac threshold saturation writing a 1 to psat or psat_ambient will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1

STATUS flags are reset with reading from STATUS address, or with writing 1 to dedicated bits of STATUS address.

CDATAL Register (0x94)

Figure 36:
CDATAL Register

0x94: CDATAL				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	CDATAL	0	RO	Low Byte of C Channel Data. If pcap_calib is active, then low byte of this result is stored here

CDATAH Register (0x95)

Figure 37:
CDATAH Register

0x95: CDATAH				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	CDATAH	0	RO	High Byte of C Channel Data. If pcap_calib is active, then high byte of this result is stored here

RDATAL Register (0x96)

Figure 38:
RDATAL Register

0x96: RDATAL				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	RDATAL	0	RO	Low Byte of R Channel Data.

RDATAH Register (0x97)

Figure 39:
RDATAH Register

0x97: RDATAH				
Field	Name	Reset	Type	Description
7:0	RDATAH	0	RO	High Byte of R Channel Data.

GDATAL Register (0x98)

Figure 40:
GDATAL Register

0x98: GDATAL				
Field	Name	Reset	Type	Description
7:0	GDATAL	0	RO	Low Byte of G Channel Data.

GDATAH Register (0x99)

Figure 41:
GDATAH Register

0x99: GDATAH				
Field	Name	Reset	Type	Description
7:0	GDATAH	0	RO	High Byte of G Channel Data.

BDATAL Register (0x9A)

Figure 42:
BDATAL Register

0x9A: BDATAL				
Field	Name	Reset	Type	Description
7:0	BDATAL	0	RO	Low Byte of B Channel Data.

BDATAH Register (0x9B)

Figure 43:
BDATAH Register

0x9B: BDATAH				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	BDATAH	0	RO	High Byte of B Channel Data.

PDATA Register (0x9C)

Figure 44:
PDATA Register

0x9C: PDATA				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	PDATA	0	RO	Prox ADC Data MSB 9:2

CFG2 Register (0x9F)

Figure 45:
CFG2 Register-ALS Gain

0x9F: CFG2				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	Reserved	0	RW	Reserved. Set to 0.
2	againl	1	RW	This is the LSB of gain_als (gain_als[0]) Overall ALS Gain Control. If this bit is set to 0 then all gains are divided by 2 (except, in case ltf_gainmax is set).
1:0	Reserved	0	RW	Reserved. Set to 0.

Figure 46:
ALS Attenuation Settings

ALS Gain Settings			
Gain	**again[1]**	**again[0]**	**againl**
	0x90.1	**0x90.0**	**0x9F.2**
1	0	0	1
4	0	1	1
16	1	0	1
64	1	1	1

CFG3 Register (0xAB)

Figure 47:
CFG3 Register

<table>
<tr><th colspan="8">0xAB: CFG3</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="4">Description</th></tr>
<tr><td>7</td><td>int_read_clear</td><td>0</td><td>RW</td><td colspan="4">If set to 1, interrupt flags in STATUS register (0x93) are reset after I^2C reads to the STATUS register; otherwise the interrupt flags will not be reset.</td></tr>
<tr><td>6:5</td><td>Reserved</td><td>0</td><td>R, SC</td><td colspan="4">Reserved. Set to 0.</td></tr>
<tr><td rowspan="7">4</td><td rowspan="7">sai</td><td rowspan="7">0</td><td rowspan="7">RW</td><td colspan="4">Sleep After Interrupt: Power down the device at the end of the proximity/ALS cycle if an interrupt has been generated.
Note that SAI does not modify any register bits directly, it rather uses the interrupt signal to turn OFF the oscillator.</td></tr>
<tr><td>PON</td><td>SAI</td><td>INT (low active)</td><td>Oscillator</td></tr>
<tr><td>0</td><td>x</td><td>x</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>x</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF (SAI induced sleep)</td></tr>
<tr><td colspan="4">The way to “wake up” the device from SAI-sleep is by clearing the interrupt register 0x93.</td></tr>
<tr><td>3:0</td><td>Reserved</td><td>0</td><td>RW</td><td colspan="4">Reserved. Set to 0.</td></tr>
</table>

POFFSET_L Register (0xC0)

Figure 48:
POFFSET_L Register

0xC0: POFFSET_L				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	poffset_l	0	R, SC	Offset compensation for proximity channel (magnitude)

POFFSET_H Register (0xC1)

Figure 49:
POFFSET_H Register

0xC1: POFFSET_H				
Field	**Name**	**Reset**	**Type**	**Description**
0	poffset_h	0	R, SC	Offset compensation for proximity channel (sign)

CALIB Register (0xD7)

Figure 50:
CALIB Register

0xD7: CALIB				
Field	**Name**	**Reset**	**Type**	**Description**
7:6	Reserved	0	RO	Reserved. Set to 0.
5	electrical_calibration	0	RW_SM	If set, do electrical offset calibration (diodes disabled) instead of optical. Otherwise, do optical calibration. In either case, the result is stored in the POFFSET_L/H registers. This flag is cleared after calibration is completed This flag is redundant, software could just: set gdiode_disab=0xf set concap_intinn=1 start calibration However, since electrical calibration is done automatically at the first time PON gets asserted, the function is there anyway, so it's made availabe to the user here.
4:1	Reserved	0	WS_SC	Reserved. Set to 0.
0	start_offset_calib	0	RW_SM	Start Offset Calibration. The result is stored in the POFFSET registers. The calib_finished flag is asserted afterwards. Calibration can be stopped by writing a 0 to this bit.

CALIBCFG Register (0xD9)

Figure 51:
CALIBCFG Register

<table>
<tr><th colspan="5">0xD9: CALIBCFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="11">7:5</td><td rowspan="11">binsrch_target</td><td rowspan="11">'h2</td><td rowspan="11">RW</td><td colspan="2">ADC target during binary search</td></tr>
<tr><td>Value</td><td>Target</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>3</td></tr>
<tr><td>3</td><td>7</td></tr>
<tr><td>4</td><td>15</td></tr>
<tr><td>5</td><td>31</td></tr>
<tr><td>6</td><td>63</td></tr>
<tr><td>7</td><td>127</td></tr>
<tr><td colspan="2">Note that this target is relative to 8-bit ADC values. In the circuit, a 10-bit target is used (x4) of which the lowest 2 bits are always ignored when checking for zero during binary search and zero detection.
In hardware, this defines a mask of which bits to ignore when comparing to zero. E.g. binsrch_target=4 (target=15) means that values from the ADC are AND'ed with 0xffc0 before comparing to zero. Only values 16 or larger are taken as positive ADC values.</td></tr>
<tr><td>4</td><td>Reserved</td><td>1</td><td>RW</td><td colspan="2">Reserved. Set to 0.</td></tr>
</table>

<table>
<tr><th colspan="6">0xD9: CALIBCFG</th></tr>
<tr><th>Field</th><th>Name</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="11">2:0</td><td rowspan="11">prx_data_avg</td><td rowspan="11">0</td><td rowspan="11">R_PUSH</td><td colspan="2">Prox data calculation is done by averaging consecutive windows of constant size. At the end of the window, PDATA is updated. Typical use case is HRM measurement</td></tr>
<tr><td>Value</td><td>Window Size</td></tr>
<tr><td>0</td><td>disable</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>3</td><td>8</td></tr>
<tr><td>4</td><td>16</td></tr>
<tr><td>5</td><td>32</td></tr>
<tr><td>6</td><td>64</td></tr>
<tr><td>7</td><td>128</td></tr>
<tr><td colspan="2">Out to be useful, we will reset this bit to zero in the production version.</td></tr>
</table>

CALIBSTAT Register (0xDC)

Figure 52:
CALIBSTAT Register

0xDC: CALIBSTAT				
Field	**Name**	**Reset**	**Type**	**Description**
0	calib_finished	0	R/W	Offset calibration has finished. Clear bit by writing '1' to it. Bit generates interrupt if cien is asserted.

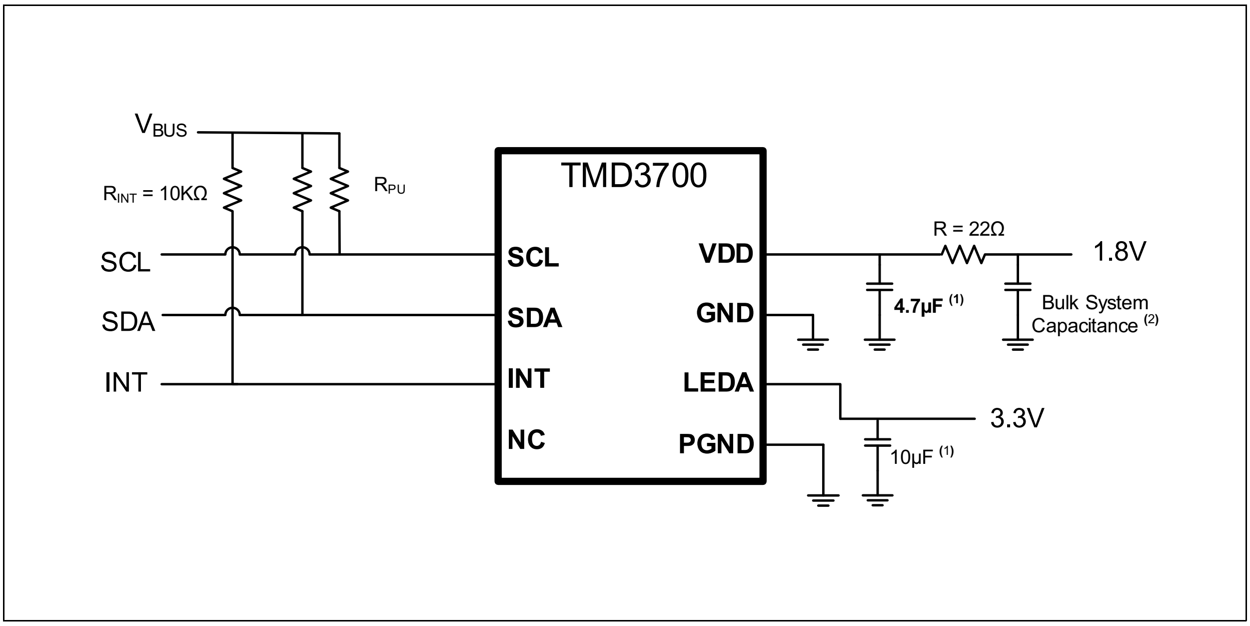
INTENAB Register (0xDD)

Figure 53:
INTENAB Register

0xDD: INTENAB				
Field	**Name**	**Reset**	**Type**	**Description**
7	asien	0	RW	Writing '1' to this bit enables asat interrupt.
6	psien	0	RW	Writing '1' to this bit enables psat
5	pien	0	RW	Writing '1' to this bit enables prox interrupt.
4	aien	0	RW	Writing '1' to this bit enables als interrupt.
3	cien	0	RW	Writing '1' to this bit enables calibration interrupt.

Application Information

Figure 54:
Typical Application Hardware Circuit

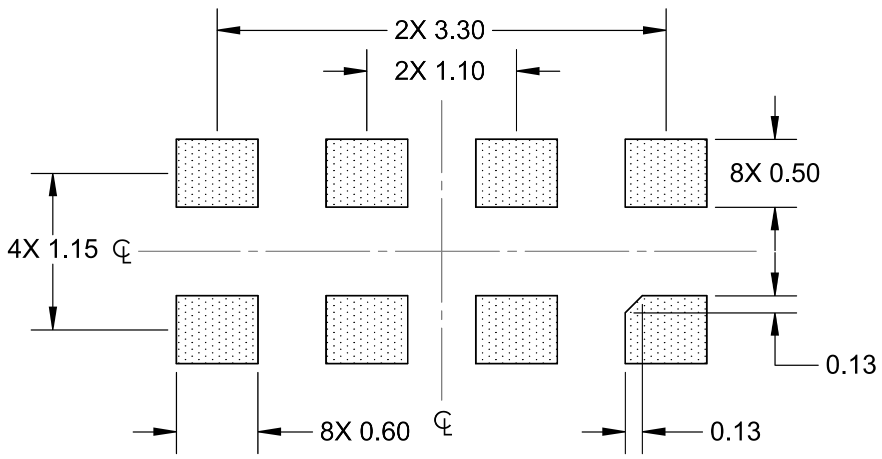


Note(s):

1. Place the 4.7µF and 10µF capacitors as close as possible to the module.
2. The bulk capacitor can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind. In systems with a clean power supply the 4.7µF and 22Ω resistor may not be needed.
3. The value of the I^2C pull up resistors R_{PU} should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
4. GND and PGND should be connected to the same solid ground plane as close to the device as possible.

PCB Pad Layout

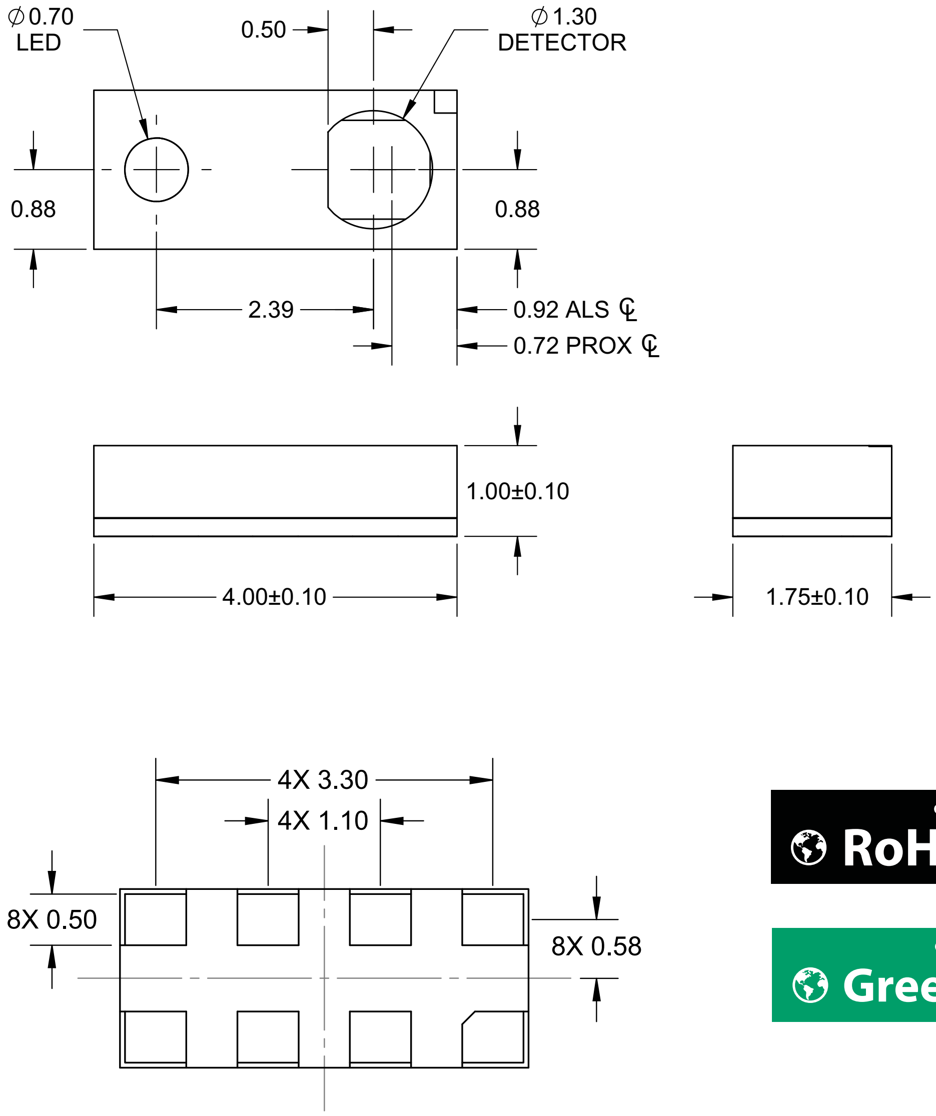
Figure 55:
Recommended PCB Pad Layout



Recommended PCB Pad Layout

Packaging Mechanical Data

Figure 56:
Package Drawing

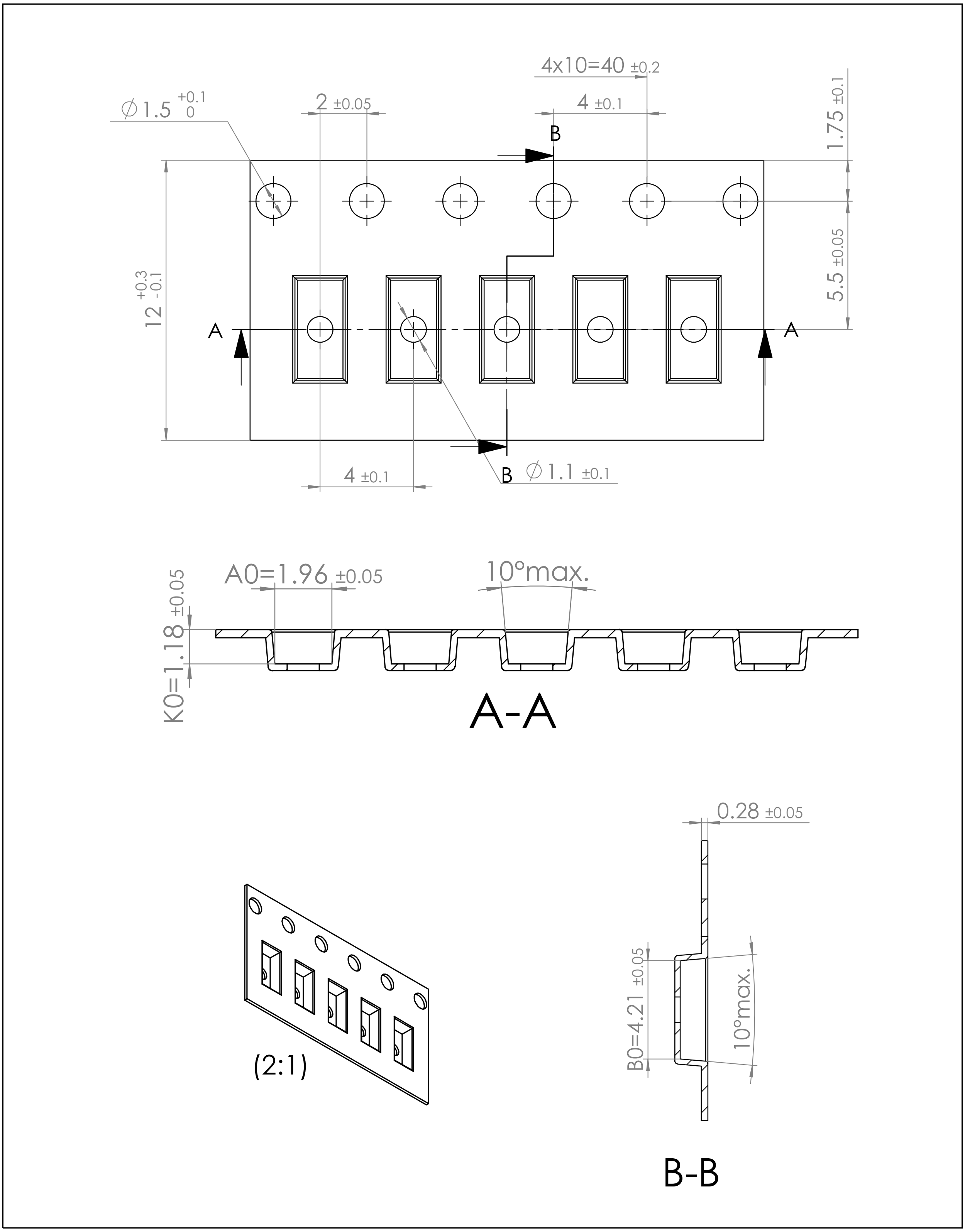


Note(s):

1. All linear dimensions are in millimeters.
2. The ALS detector is centered in the opening within a tolerance of ±0.03 millimeters.
3. Contact finish is AU.
4. This drawing is subject to change without notice.

Tape & Reel Information

Figure 57:
Tape & Reel Information



Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Soldering & Storage Information

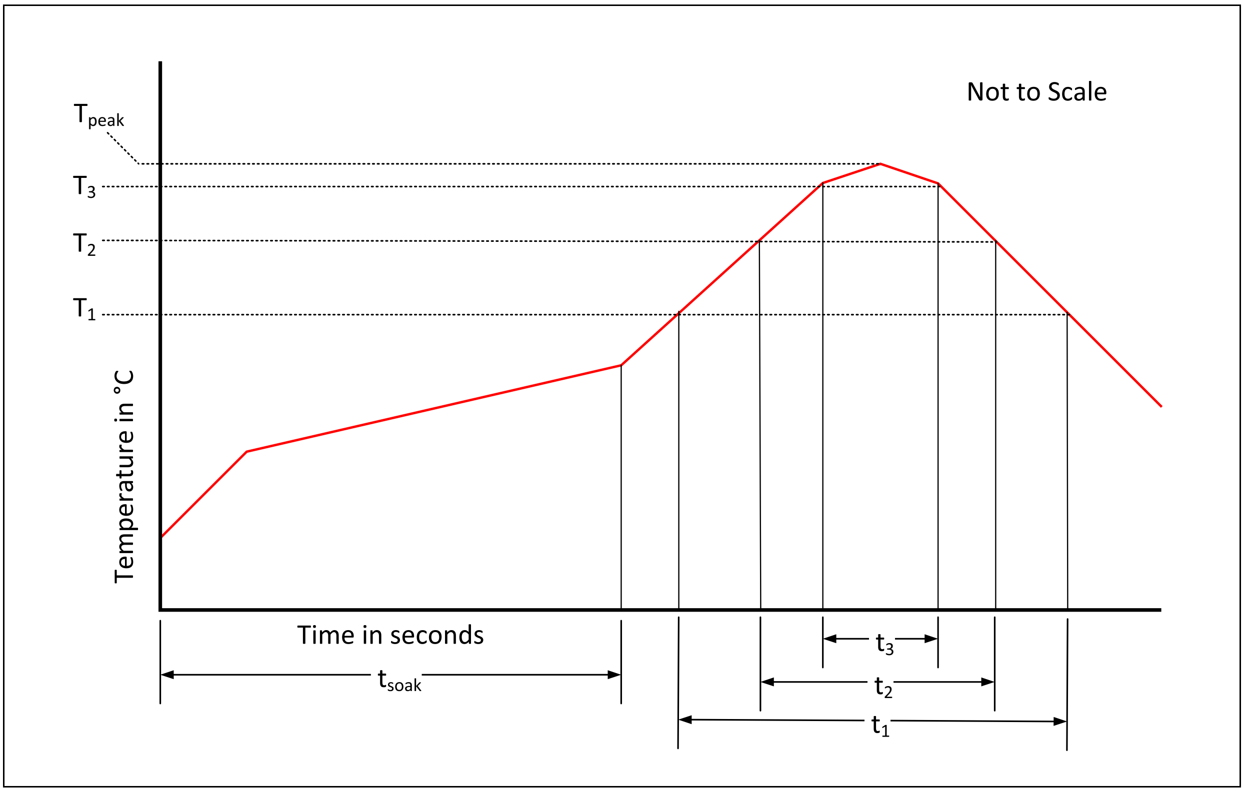
The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 58:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60s
Time above 230°C (T_2)	t_2	Max 50s
Time above T_{peak} – 10 °C (T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/s

Figure 59:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 60:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD37003	1.8V	39h	Tape & Reel (13")	10000 pcs/reel
TMD37003M	1.8V	39h	Tape & Reel (7")	1000 pcs/reel
TMD37007 (1)	1.8V	29h	Tape & Reel (13")	10000 pcs/reel

Note(s):

1. Consult factory for availability of secondary address versions.

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Revision Information

Changes from 1-01 (2016-Jun-27) to current revision 1-02 (2016-Aug-19)	Page
Removed POFFEST Magnitude and POFFSET Sign registers	
Updated Figure 7	5
Updated Figure 17	12

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide