PIC24FJ128GB204 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ128GB204 family devices that you have received conform functionally to the current Device Data Sheet (DS30005009**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ128GB204 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ128GB204 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		B3
PIC24FJ128GB204	0x4C5B	0x04
PIC24FJ128GB202	0x4C5A	
PIC24FJ64GB204	0x4C59	
PIC24FJ64GB202	0x4C58	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXGA2/GB2 Families Flash Programming Specification"* (DS30000510) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				B3
UART	Break Character Transmission	1.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.	X
A/D Converter	Band Gap Voltage Measurement	2.	Incorrect Band Gap Reference (VBG/2) measurement with the A/D Converter at full speed.	X
Input Capture	Synchronous Cascade mode	3.	Even numbered timer does not reset on a source clock rollover in synchronous cascaded operation.	X
Output Compare 3, 4, 5 and 6	PWM mode	4.	In the scaled down timer source for the Output Compare module, the first PWM pulse may not appear on the OCx pin.	X
CTMU	Edge Enable bit (EDGEN)	5.	The Edge Enable bit (EDGEN) generates a glitch on the CTEDx input.	X
UART1 and UART2	SmartCard/ Interrupt	6.	Early interrupt for the last byte in T = 1 mode.	X
UART1 and UART2	SmartCard/ Guard Time Counter	7.	Guard Time Counter (GTC) is off by one count in T = 0 and T = 1 modes.	X
POR/BOR	Reset	8.	If the Brown-out Reset (BOR) is disabled, the part may fail to come out of the Reset state during the VDD power-down and the subsequent power-up condition.	X
POR/BOR	Reset	9.	When the BOR is disabled, the part may not start at the minimum VDD specification.	X
Output Compare	Sync Mode	10.	The Output Compare (OC) module does not get synchronized with the source timer in Sync mode when the source timer is running with an external clock.	X
Input Capture	Sync Mode	11.	The Input Capture (IC) module does not get synchronized with the source timer in Sync mode when the source timer is running with an external clock.	X
UART1 and UART2	SmartCard/ Receive	12.	UART receive interrupt is asserted early.	X
UART1 and UART2	SmartCard/ Interrupt	13.	Clearing a UxSCINT register status bit clears all status bits.	X
UART1 and UART2	SmartCard/ Waiting Time Counter	14.	Waiting time is extended by 11 ETUs when WTCx > 10.	X
SPI	Master Mode	15.	Transmit watermark interrupt is not asserted in Master mode with more than one data packet in FIFO.	X
I^2C	Slave Mode	16.	Bus data corruption with multiple slaves on bus.	X
I^2C	Slave Mode	17.	With Slave in Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if Address Hold Enable (AHEN) and Data Hold Enable (DHEN) are disabled (AHEN = 0 and DHEN = 0).	X
I^2C	Slave Mode	18.	In 10-Bit Addressing mode with Address Hold Enable (AHEN = 1), the Acknowledge Time Status bit (ACKTIM) is not asserted only for the upper address byte (A9 and A8).	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				B3
I^2C	Address Hold	19.	In Slave mode when AHEN = 1 (Address Hold Enabled), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X
I^2C	Data Hold	20.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X
I^2C	Slave Mode	21.	In Slave mode with general call and address hold enabled, when the general call address is received, the slave interrupt is not asserted after the 8th clock.	X
Output Compare (OC)	Cascade Mode	22.	In Cascade mode with the Output Compare Data register (OCxR) and Secondary Data register (OCxRS) of the even OC module set to zero, then cascaded OC does not generate output.	X
SPI	Slave Mode	23.	In Slave mode, the RX watermark interrupt does not wake the device from Sleep, which causes loss of the first few receive bytes.	X
SPI	Audio PCM/DSP	24.	SPI module follows the Right Justified mode of transmission and reception in PCM/DSP mode.	X
SPI	Slave Mode Audio	25.	In Slave mode, the Most Significant bit (MSb) is missed in Left and Right Justified modes.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA<11>), to be cleared instead of the TRMT bit (UxSTA<8>) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

B3							
X							

2. Module: A/D Converter

Incorrect $V_{BG}/2$ voltage measurement of the A/D Converter at full speed.

When the A/D Converter is converting at full speed (500 ksps for 10-bit and 200 ksps for 12-bit), the A/D Converter count may not match the $V_{BG}/2$ voltage.

Work around

The A/D Converter clock should be lowered to below 100 ksps (in 12-bit mode) to read the correct value of the $V_{BG}/2$ voltage. In 10-bit mode, the clock must be lowered to below 200 ksps.

Affected Silicon Revisions

B3							
X							

3. Module: Input Capture

The even numbered timer does not reset on a source clock rollover in Synchronous Cascaded mode operation.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules) form a single 32-bit module. In Synchronous Cascaded mode (IC32 = 1, ICTRIG = 0 and the SYNCSEL<4:0> bits are not equal to 0h), both timers, ICyTMR:ICxTMR, must reset on a Sync_trig input from the 32-bit source timers, but only the odd timer (ICxTMR) is getting reset on a Sync_trig input.

Work around

None.

Affected Silicon Revisions

B3							
X							

4. Module: Output Compare 3, 4, 5 and 6

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS<1:0> (TxCON<5:4>).

Work around

- Configure the prescaler for the source timer to 1:1 for Output Compare 3, 4, 5 and 6.
- The Output Compare 1 or 2 module can be used. The scaled down timer (1:8, 1:64 or 1:256) can be used as a source for the Output Compare 1 and 2 modules.

Affected Silicon Revisions

B3							
X							

5. Module: CTMU

The Edge Enable bit, EDGEN (CTMUCON1<11>), generates a glitch on the CTEDx input.

Enabling the edges (EDGEN = 1) generates a glitch (edge):

- If the CTMU External Edge Input (CTEDx) is set for a falling edge and the level on this pin is low;
  or
- If CTEDx is set for a rising edge and the level on this pin is high.

Work around

None.

Affected Silicon Revisions

B3							
X							

6. Module: UART1 and UART2

This issue applies to SmartCard/ISO7816 operation.

In T = 1 mode, for the last byte and when the LAST bit is set, an interrupt shall always be generated after 22 Elementary Time Units (ETUs), irrespective of the Guard Time Interrupt Enable bit, GTCIE (UxSCINT<0>), state. The interrupt is occurring before 22 ETUs.

Work around

To use the Guard Time Counter (GTC) for T = 1 block guard time, the last byte in a message block must have the GTC value set to 11 ETUs and the GTCIE (UxSCINT<0>) bit set. The LAST bit (UxTXREG<15>) should not be set.

Affected Silicon Revisions

B3							
X							

7. Module: UART1 and UART2

This issue applies to SmartCard/ISO7816 operation.

The Guard Time Counter (GTC) is off by one count in T = 0 and T = 1 modes.

The GTC value stored in the UxGTC register is off by one count in both T = 0 and T = 1 modes. The actual guard time is, a +1 ETU more, than the value specified in the GTC<8:0> bit.

Work around

The guard time value to be programmed in the GTC<8:0> bits must be decremented by one count.

Affected Silicon Revisions

B3							
X							

8. Module: POR/BOR

If Brown-out Reset (BOR) is disabled, the part may fail to come out of the Reset state during the VDD power-down and the subsequent power-up condition.

When BOR is disabled, in extremely rare cases, the part remains in the Reset state during the VDD power-down (not till VSS), followed by the subsequent power-up condition.

Work around

There are three known work arounds for this issue:

- Always enable BOR by setting the Configuration Fuse bit, BOREN = 1 (CW3<12>).
- Use an external voltage supervisor chip on the MCLR pin to hold the MCLR low when the power supply voltage is between 1.4V and 2.0V. Release MCLR after the VDD is in the operating range.
- Make sure that VDD goes all the way to VSS before powering on.

Affected Silicon Revisions

B3							
X							

9. Module: POR/BOR

When BOR is disabled, the part may not start at the minimum VDD specification.

Work around

There are two known work arounds for this issue:

- Always enable BOR by setting the Configuration Fuse bit, BOREN (CW3<12>) = 1.
- For initial start-up, make sure that the minimum VDD is more than 2.2V. Once the device is powered, it will operate down to the minimum VDD voltage specified in the data sheet specifications. This is a typical battery-operated application with a fully charged battery installed into the application. The part will continue to operate to the data sheet specifications.

Affected Silicon Revisions

B3							
X							

10. Module: Output Compare

The Output Compare x module does not get synchronized with the source timer in Sync mode when the source timer is running with an external clock.

In Synchronous mode, the internal 16-bit counter, OCxTMR, is synchronized with TMRx. When the source clock (TMRx) to the OCx module is running on an external clock, TCS (TxCON<1>) = 1, the OCxTMR is not synchronized with TMRx.

Work around

None.

Affected Silicon Revisions

B3							
X							

11. Module: Input Capture

The Input Capture x module does not get synchronized with the source timer in Sync mode when the source timer is running with an external clock.

In Synchronous mode, the internal 16-bit counter, ICxTMR, is synchronized with TMRx. When the source clock (TMRx) to the ICx module is running on an external clock, TCS (TxCON<1>) = 1, the ICxTMR is not synchronized with TMRx.

Work around

None.

Affected Silicon Revisions

B3							
X							

12. Module: UART1 and UART2

The UARTx Receive Interrupt Flag (UxRXIF) may be asserted early, before the entire incoming data byte is received. As a result, during SmartCard operations, the data byte read from the UARTx Receive Buffer will not be valid.

Work around

None.

Affected Silicon Revisions

B3							
X							

13. Module: UART1 and UART2

Clearing any one of the interrupt status bits in the UxSCINT register (i.e., GTCIF, WTCIF, TXRPTIF or RXRPTIF) may result in clearing of all of the status bits. The status of corresponding interrupt enable bits is not affected.

Work around

Before clearing any of the UxSCINT status bits, copy the contents of the register to memory.

Affected Silicon Revisions

B3							
X							

14. Module: UART1 and UART2

When the value of the Waiting Time Counter (WTC) stored in UxWTC is greater than 10, the actual waiting time is extended by an additional 11 Elementary Time Units (ETUs). For example, when UxWTC = 11, the application will assert a waiting time of 22 ETUs.

Work around

None.

Affected Silicon Revisions

B3							
X							

15. Module: SPI

While operating in Master mode (MSTEN = 1), the Transmit Watermark interrupt is not asserted if there is more than one entry in the FIFO buffer. This means, for various modes, that the interrupt is not asserted for:

- More than one byte to be transmitted in 8-bit mode;
- More than one word to be transmitted in 16-bit mode; or
- More than one double word to be transmitted in 32-bit mode.

Work around

None.

Affected Silicon Revisions

B3							
X							

16. Module: I^2C

In applications with multiple I^2C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

B3							
X							

17. Module: I^2C

With Slave in Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if Address Hold Enable (AHEN) and Data Hold Enable (DHEN) are disabled.

The Acknowledge Time Status bit (ACKTIM) is asserted only if Address Hold Enable (AHEN) or Data Hold Enable (DHEN) is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for assertion of the Receive Buffer Full (RBF) flag.

Affected Silicon Revisions

B3							
X							

18. Module: I^2C

In 10-Bit Addressing mode with Address Hold Enable (AHEN = 1), the Acknowledge Time Status bit (ACKTIM) is not asserted only for the upper address byte (A9 and A8).

The ACKTIM bit is asserted for the lower address byte (A7 to A0).

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for assertion of the Receive Buffer Full (RBF) flag.

Affected Silicon Revisions

B3							
X							

19. Module: I²C

In Slave mode when AHEN = 1 (Address Hold Enabled), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear the ACKDT (Acknowledge Data) bit on receiving the Start bit.

Affected Silicon Revisions

B3							
X							

20. Module: I²C

In Slave mode when DHEN = 1 (Data Hold Enabled), if the ACKDT (Acknowledge Data) bit is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear the ACKDT (Acknowledge Data) bit on receiving the Start bit.

Affected Silicon Revisions

B3							
X							

21. Module: I²C

In Slave mode with general call (GCEN = 1) and address hold (AHEN = 1) enabled, when the general call address (0x00) is received, a slave interrupt is not asserted after the 8th clock.

Work around

Mask the address bits. Upon address reception, verify if it is a device/general call address and ACK address accordingly.

Affected Silicon Revisions

B3							
X							

22. Module: Output Compare (OC)

When the OC module is used in Cascade mode with the Output Compare Data register (OCxR) and Secondary Data register (OCxRS) of the even OC module set to zero, then the cascaded OC does not generate output.

In the cascaded configuration, OCy:OCx (OCy represents the even numbered modules and OCx represents the odd numbered modules) form a single 32-bit module. In such a configuration, if OCyR and OCyRS are set to zero, then the cascaded OCyTMR:OCxTMR registers do not compare with the cascaded OCyR:OCxR and OCyRS:OCxRS registers. Hence, cascaded OC does not generate any output.

Work around

None.

Affected Silicon Revisions

B3							
X							

23. Module: SPI

The RX watermark interrupt is not asserted for the first few bytes in Sleep mode when the SPI slave is configured for 8, 16 or 32-Bit Enhanced Buffer mode (MSTEN = 0, ENHBUF = 1).

The interrupt does not get asserted for any value of the buffer mask (RXMSK<5:0>). For 8-bit mode, interrupt after 32; for 16-bit mode, interrupt after 16; for 32-bit mode, interrupt after 8.

Work around

Tie the SPI clock pin to the external interrupt in the slave device. This work around has a limitation on the SPI speed of 5 MHz.

Affected Silicon Revisions

B3							
X							

24. Module: SPI

The SPI module, irrespective of master or slave configured for PCM/DSP mode, follows the Right Justified mode of transmission and reception.

Work around

None.

Affected Silicon Revisions

B3							
X							

25. Module: SPI

In Slave Left Justified or Right Justified modes, the Most Significant bit (MSb) of the data is missed.

Work around

None.

Affected Silicon Revisions

B3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30005009**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Pin Diagrams

AN9 has been removed from all 28-pin diagrams and tables. This analog channel is unimplemented in 28-pin devices.

2. Module: Timer2/3 and Timer4/5

At the beginning of the Timer2/3 and Timer4/5 section, the following bullet item:

- Timer Operation during Idle and Sleep modes

has been changed to:

- Timer Operation during Idle mode

3. Module: Inter-Integrated Circuit (I^2C)

In Register 17-2, the following note has been added to the SDAHT bit description:

Note 1: This bit must be set to '0' for 1 MHz operation.

4. Module: Inter-Integrated Circuit (I^2C)

Equation 17-1 has been updated. The changes are shown below in **bold**:

EQUATION 17-1: COMPUTING BAUD RATE RELOAD VALUE(1)

$$I2CxBRG = \left(\left(\frac{1}{F_{SCL}} - \textbf{\textit{Delay}}\right) \times \frac{F_{CY}}{2}\right) - 2$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

5. Module: 12-Bit A/D Converter with Threshold Detect

In Figure 25-1, Note 1 has been updated to include AN9:

Note 1: **AN9** through AN12 are implemented on 44-pin devices only.

6. Module: 12-Bit A/D Converter with Threshold Detect

In Register 25-6, AN9 has been added to Note 2 to indicate that it is unimplemented in 28-pin devices.

7. Module: Memory Organization

In Table 4-4, the CN0PDE (CNPD1<0>), CN1PDE (CNPD1<1>), CN0PUE (CNPU1<0>) and CN1PUE (CNPU1<1>) bits are unimplemented.

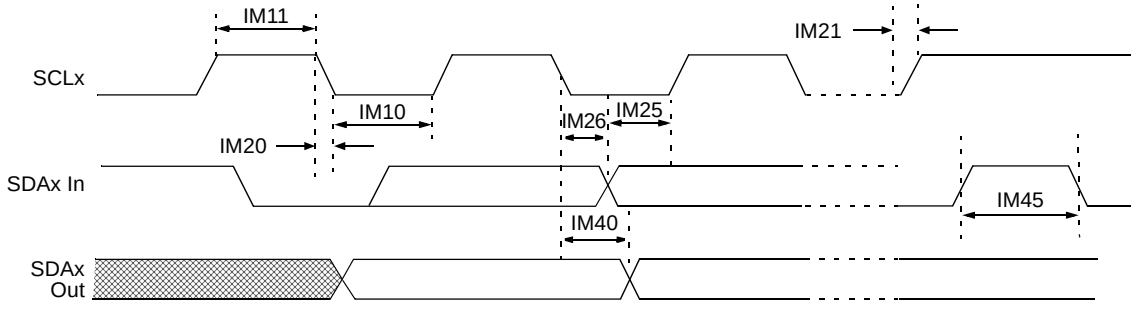
8. Module: Power-Saving Features

In Table 10-2, Note 2 has been removed because it does not apply.

9. Module: I²C

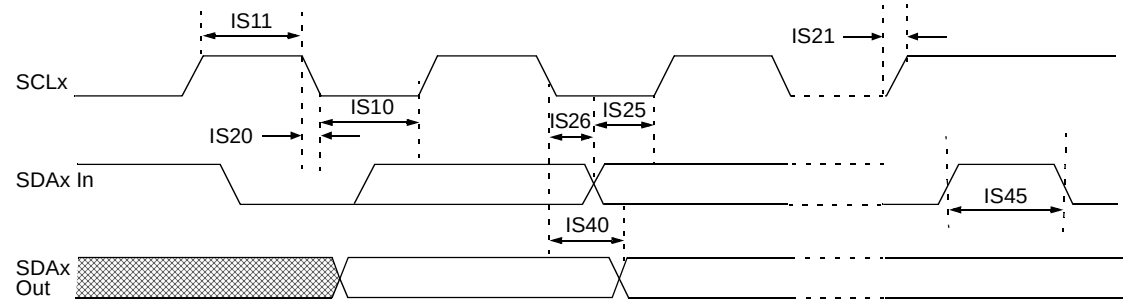
Figure 33-14 and Figure 33-16 are modified as shown in the figures below.

FIGURE 33-14: I²C BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 33-2 for load conditions.

FIGURE 33-16: I²C BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



10. Module: I²C

In Register 17-3: I2CxSTAT, the S (I2CxSTAT<3>) and P (I2CxSTAT<4>) bits are read-only.

11. Module: RTCC

In Section 22.1, the following information is added:

If the RTCC is running from the external VBAT supply pin, the SOSC or LPRC clock source must be used. The external oscillator will not function in VBAT modes.

12. Module: Device Overview

In Figure 1-1: PIC24FJ128GB204 Family General Block Diagram, the BGBUF1 and BGBUF2 pins are removed.

13. Module: SPI

Section 16.3 changes to: **"Enhanced Master Mode"**.

Section 16.4 changes to: **"Enhanced Slave Mode"**.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2014)

Initial release of this document; issued for silicon revision B3.

This version includes the following silicon issues 1 (UART), 2 (A/D Converter), 3 (Input Capture), 4 (Output Compare 3, 4, 5 and 6), 5 (CTMU), 6-7 (UART1 and UART2), 8-9 (POR/BOR), 10 (Output Compare) and 11 (Input Capture).

Rev B Document (1/2015)

Adds silicon issues 12 through 14 (UART1 and UART2), 15 (SPI) and 16 (I^2C).

Updates the title of existing silicon issues 6 and 7 as "UART1 and UART2", in accordance with standard documentation practice. The actual issues themselves, as they relate to the SmartCard/ISO7816 functionality of the UART, remain unchanged.

Adds data sheet clarifications 1 (Triple Comparator) and 2 (Packaging).

Rev C Document (6/2015)

Adds silicon issues 17 (I^2C) and 18 (I^2C).

Removes data sheet clarifications 1 (Triple Comparator) and 2 (Packaging).

Adds new data sheet clarifications 1 (Pin Diagrams), 2 (Timer2/3 and Timer4/5), 3 (Inter-Integrated Circuit (I2C)), 4 (Inter-Integrated Circuit (I2C)), 5 (12-Bit A/D Converter with Threshold Detect), 6 (12-Bit A/D Converter with Threshold Detect) and 7 (Memory Organization).

Rev D Document 7/2015

Adds new data sheet clarification 8 (Power-Saving Features).

Rev E Document 2/2017

Adds silicon issues 19 (I^2C), 20 (I^2C), 21 (I^2C), 22 (Output Compare (OC)), 23 (SPI), 24 (SPI) and 25 (SPI).

Adds new data sheet clarifications 9 (I^2C), 10 (I^2C), 11 (RTCC), 12 (Device Overview) and 13 (SPI).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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