Advantech

AQD-SD3L4GN16-MQ
Datasheet

Rev. 0.0

2014-03-8

Description

AQD-SD3L4GE16-MG is a DDR3L SO DIMM high-speed, low power memory module that use 16 pcs of 256Mx8bits DDR3 low voltage SDRAM in FBGA package and a 2K bits serial EEPROM on a 204-pin printed circuit board. AQD-SD3L4GN16-MQ is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

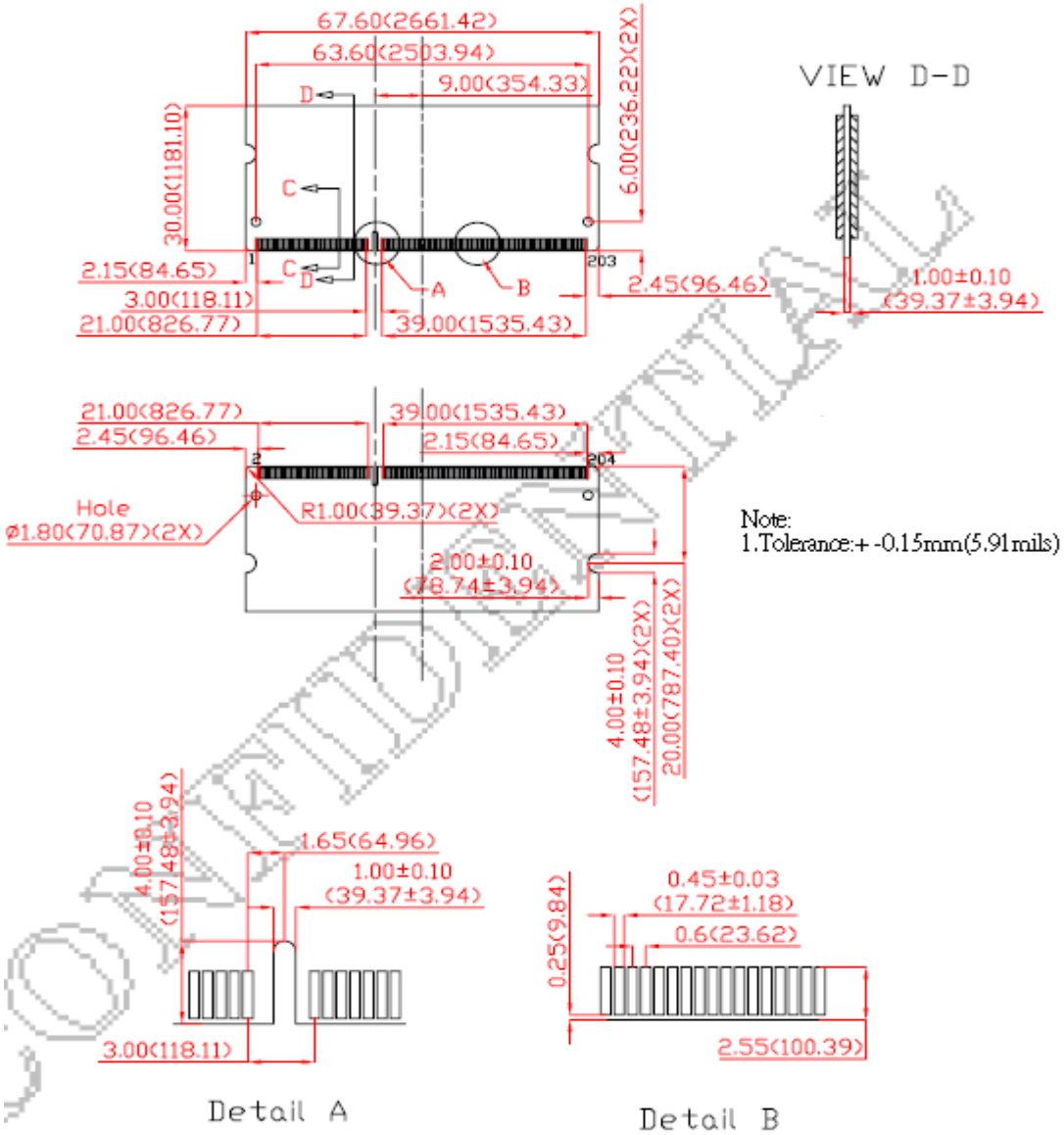
Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.28V~1.45V) Power supply
- JEDEC standard 1.5V(1.425V~1.575V) Power supply
- VDDQ=1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)
- Clock Freq: 800MHZ for 1600MT/s.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS):
- 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL)
- = 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
  Asynchronous reset
- PCB edge connector treated with 30u” Gold-Plating

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0 &ODT1	On-die termination control line
/S0 &/S1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
$V_{REF}DQ$	DQ reference supply
$V_{REF}CA$	Command/address reference supply
$V_{DD}SPD$	SPD EEPROM power supply
SA0~SA1	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	DRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



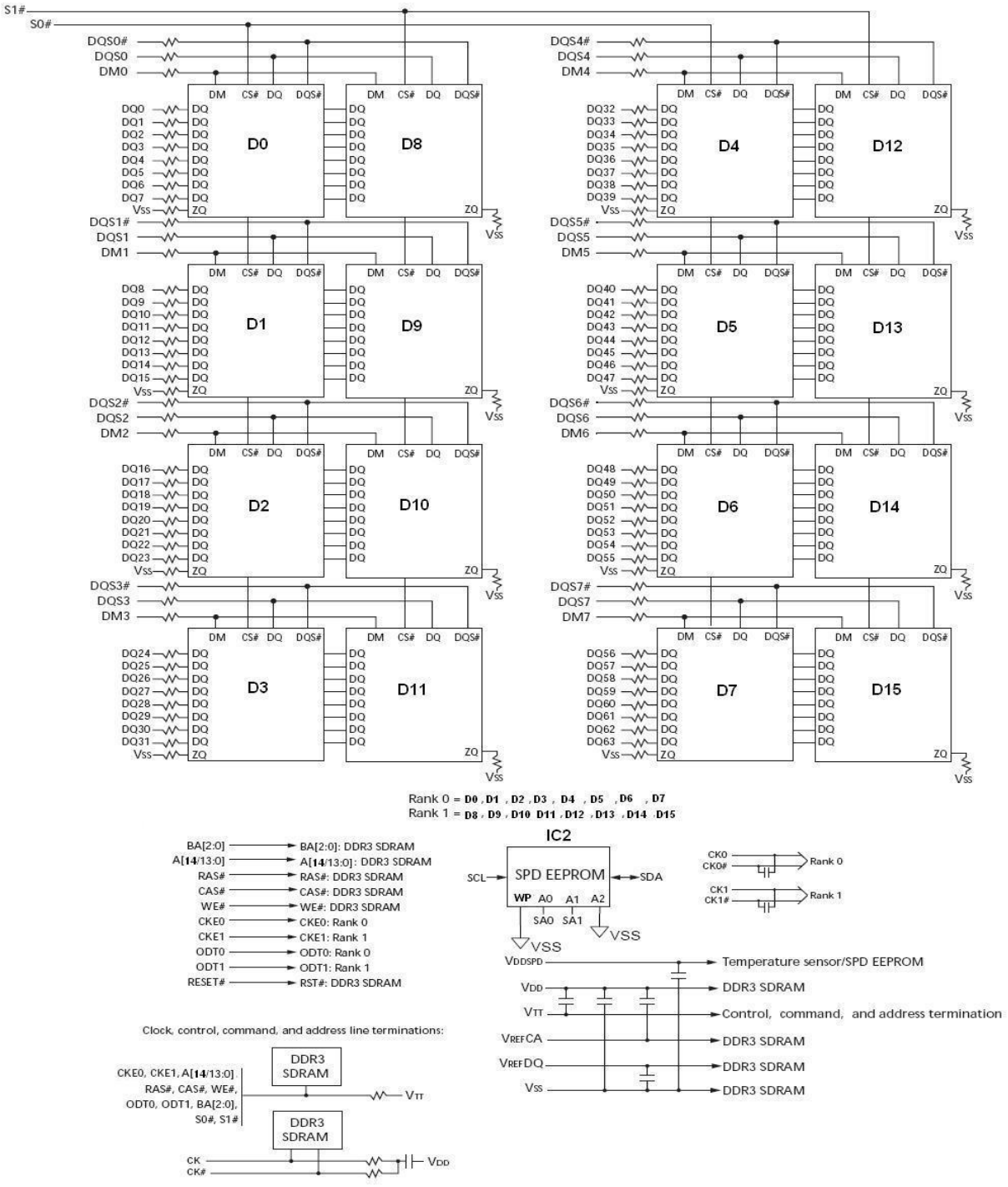
Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	41	DQ17	81	VDD	121	/S1	161	VSS	201	SA1
02	VSS	42	DQ21	82	VDD	122	NC	162	VSS	202	SCL
03	VSS	43	VSS	83	A12/BC	123	VDD	163	DQ48	203	VTT
04	DQ4	44	VSS	84	A11	124	VDD	164	DQ52	204	VTT
05	DQ0	45	/DQS2	85	A9	125	TEST	165	DQ49		
06	DQ5	46	DM2	86	A7	126	VREFCA	166	DQ53		
07	DQ1	47	DQS2	87	VDD	127	VSS	167	VSS		
08	VSS	48	VSS	88	VDD	128	VSS	168	VSS		
09	VSS	49	VSS	89	A8	129	DQ32	169	/DQ56		
10	/DQS0	50	DQ22	90	A6	130	DQ36	170	DM6		
11	DM0	51	DQ18	91	A5	131	DQ33	171	DQS6		
12	DQS0	52	DQ23	92	A4	132	DQ37	172	VSS		
13	VSS	53	DQ19	93	VDD	133	VSS	173	VSS		
14	VSS	54	VSS	94	VDD	134	VSS	174	DQ54		
15	DQ2	55	VSS	95	A3	135	/DQS4	175	DQ50		
16	DQ6	56	DQ28	96	A2	136	DM4	176	DQ55		
17	DQ3	57	DQ24	97	A1	137	DQS4	177	DQ51		
18	DQ7	58	DQ29	98	A0	138	VSS	178	VSS		
19	VSS	59	DQ25	99	VDD	139	VSS	179	VSS		
20	VSS	60	VSS	100	VDD	140	DQ38	180	DQ60		
21	DQ8	61	VSS	101	CK0	141	DQ34	181	DQ56		
22	DQ12	62	/DQ3	102	CK1	142	DQ39	182	DQ61		
23	DQ9	63	DM3	103	/CK0	143	DQ35	183	DQ57		
24	DQ13	64	DQ3	104	/CK1	144	VSS	184	VSS		
25	VSS	65	VSS	105	VDD	145	VSS	185	VSS		
26	VSS	66	VSS	106	VDD	146	DQ44	186	/DQS7		
27	/DQS1	67	DQ26	107	A10/AP	147	DQ40	187	DM7		
28	DM1	68	DQ30	108	BA1	148	DQ45	188	DQS7		
29	DQS1	69	DQ27	109	BA0	149	DQ41	189	VSS		
30	/RESET	70	DQ31	110	/RAS	150	VSS	190	VSS		
31	VSS	71	VSS	111	VDD	151	VSS	191	DQ58		
32	VSS	72	VSS	112	VDD	152	/DQS5	192	DQ62		
33	DQ10	73	CKE0	113	/WE	153	DM5	193	DQ59		
34	DQ14	74	CKE1	114	/S0	154	DQS5	194	DQ63		
35	DQ11	75	VDD	115	/CAS	155	VSS	195	VSS		
36	DQ15	76	VDD	116	ODT0	156	VSS	196	VSS		
37	VSS	77	NC	117	VDD	157	DQ42	197	SA0		
38	VSS	78	A15	118	VDD	158	DQ46	198	NC		
39	QC16	79	BA2	119	A13	159	DQ43	199	VDDSPD		
40	DQ20	80	A14	120	ODT1#	160	DQ47	200	SDA		

/S1,ODT1,CKE1：Used for dual-rank UDIMMs; NC on single-rank UDIMMs.
CK1 and /CK1：Used for dual-rank UDIMMs; not used on single-rank UDIMMs but terminated.

4GB, 2Gbx16 Module(2 Rank x8)



Notes: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1 percent resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	-10 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.975	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.975	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575	V	
Supply voltage for Output	VDDQ	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575	V	
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.35V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.5V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	VIH(AC)	1.35V	VREF+0.160	-	-	V	
		1.5V	VREF+0.175	-	-	V	
AC Input Logic Low	VIL(AC)	1.35V	-	-	VREF-0.160	V	
		1.5V	-	-	VREF-0.175	V	
DC Input Logic High	VIH(DC)	1.35V	V_{REF}+0.09	-	VDD	V	
		1.5V	V_{REF}+0.1	-	VDD	V	
DC Input Logic Low	VIL(DC)	1.35V	VSS	-	V_{REF}-0.09	V	
		1.5V	VSS	-	V_{REF}-0.1	V	

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

IDD Specification parameters Definition - 4GB (2 Rank x8)

Parameter	Symbol	DDR3 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	440	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	528	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	144	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	256	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	256	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	304	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	304	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1256	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1000	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1240	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1760	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(4xnm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3 1600		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	1.25	-	ns
CK high-level width	tCH	0.47	0.53	tCK
CK low-level width	tCL	0.47	0.53	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK
DQ low-impedance time from CK, /CK	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	225	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS	10	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH	45		ps
DQ and DM input pulse width for each input	tDIPW	360	-	ps
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential Read postamble	tRPST	0.3	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
DQS, /DQS Write postamble	tWPST	0.3	-	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	-450	225	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	225	ps
DQS, /DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	Max (4tck, 7.5ns)	-	
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	4	-	tCK
/CAS to /CAS command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tck		nCK

Active to active command period for 1KB page size	tRRD	Max (4tck, 7.5ns)	-	ns
Speed		**DDR3 1600**		**Unit**
Parameter	**Symbol**	**Min**	**Max**	
Active to active command period for 2KB page size	tRRD	Max (4tck, 6ns)	-	
Four Activate Window for 1KB page size	tFAW	30	-	ns
Power-up and RESET calibration time	tZQinitl	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQcs	64	-	tCK
Exit self refresh to commands not requiring a locked DLL	tXS	Max (5tCK, tRFC+10ns)	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tCK
Internal read to precharge command delay	tRTP	Max (4tck, 7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCK(min)+1tCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	Max (3tCK, 6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	Max (3tCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
ODT turn-off	tAOF	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

AQD-SD3L4GE16-MG Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	2Gb 8banks	03
5	SDRAM Addressing	ROW:15, Column:10	19
6	Reserved	1.35V and 1.5V	02
7	Module Organization	2Rank / x8	09
8	Module Memory Bus Width	Non ECC 64bit	03
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8, 9,10,11	FE
15	CAS Latencies Supported, Most Significant Byte	6, 7, 8, 9,10,11	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	35ns	18
23	Minmum Active to Active/Refresh Time (tRCmin)	48.125ns	81
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	160ns	00
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	160ns	05
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	ASR / 85℃~95℃ 2X refresh rate /95℃	05

32	Module Thermal Sensor	Non Thermal Sensor	00
33	SDRAM Device Type	-	00
34-59	Reserved, General Section	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	-	11
62	Reference Raw Card Used	Raw Card F Revision 0	05
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117	Module Manufacturer ID Code, Least Significant Byte	ADATA	04
118	Module Manufacturer ID Code, Most Significant Byte	ADATA	CB
119	Module Manufacturing Location	*Note: 1	-
120	Module ID: Module Manufacturing Date(Year)	*Note: 2	-
121	Module ID: Module Manufacturing Date(Week)	*Note: 3	-
122-125	Module ID : Module Serial Number	*Note: 4	-
126	Cyclical Redundancy Code	CRC-CCITT(LOW)	2F
127	Cyclical Redundancy Code	CRC-CCITT(HIGH)	97
128-145	Module Part Number	*Note: 5	-
146-147	Revision Code	-	00
148	DRAM Manufacturer ID Code		00
149	DRAM Manufacturer ID Code		00
150-151	Manufacturer Specific Data	-	00
152-163	Manufacturer's Specific Data (Working Order Number)	*Note: 5	-
164-175	Manufacturer's Specific Data (SPD Naming Number)	*Note: 6	-
176-255	Open for customer use	*Note: 7	-

***Note :**

1. Byte 119 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Byte 120 -- Module manufacturing date by year (YY).
3. Byte 121 -- Module manufacturing date by week (WW).
4. Bytes 122~125 -- Module Serial Number.
5. Bytes 128~145 -- Manufacturer Part Number by module part number ,
   (Unused digits are coded as ASCII blanks (20h)).
6. Bytes 152~163 -- Manufacturer's Specific Data by working order number.
   (Unused digits are coded as 00h.)
7. Bytes 164~175 -- Manufacturer's Specific Data by SPD naming number.
   (Unused digits are coded as 00h.)
8. Bytes 176~255 --These bytes are undefined and can be used for A-DATA's own purpose.
   Digits are coded as 00h except 218=ADh now.